PCI-DAS1000

Specifications

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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Specification
A/D converter type	*7800*
Resolution	12 bits
Number of channels	8 differential or 16 single-ended, software selectable
Input ranges	±10 V, ±5 V, ±2.5 V, ±1.25 V, 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V. Fully programmable
Polarity	Unipolar/bipolar, software selectable
A/D pacing	Programmable: Internal counter or external source (A/D External Pacer, positive or negative edge selectable by software), or software polled
Burst mode	Software selectable option, rate = 4 µs
A/D trigger sources	External digital (A/D External Trigger)
A/D triggering modes	Digital: Software enabled, rising edge**,** hardware trigger Pre-trigger: Unlimited pre- and post-trigger samples. Total # of samples must be > 512.
Data transfer	From 1024 sample FIFO via REPINSW, interrupt or software polled
A/D conversion time	*3 µs*
Throughput	250 kHz
Relative accuracy	±1.5 LSB
Differential linearity error	±0.75 LSB
Integral linearity error	±0.5 LSB typ, ±1.5 LSB max
Gain error (relative to calibration reference)	± 0.02% of reading, max
No missing codes guaranteed	*12 bits*
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM
Gain drift (A/D specs)	*±6 ppm/°C*
Zero drift (A/D specs)	*±1 ppm/°C*
Common mode range	±10 V
CMRR @ 60 Hz	70 dB
Input leakage current	*200 nA*
Input impedance	*10 MOhms, min*
Absolute maximum input voltage	*Channels 1-15: -40 V to +55 V power on or off; Channel 0 : ±15 V*
Noise distribution	Rate = 1-250 kHz, average % ±2 bins, average % ±1 bin, average # bins
	All bipolar ranges: 100% / 99.5% / 4 bins All unipolar ranges:100% / 99% / 5 bins

Digital input/output

Table 2. DIO specifications

Parameter	Specification
Digital type	*82C55A*
Configuration	*2 banks of 8, 2 banks of 4, programmable by bank as input or output*
Number of channels	*24 I/O (FIRSTPORTA 0 through FIRSTPORTC 7)*
Output high	*3.0 volts, min @ -2.5 mA*
Output low	*0.4 volts, max @ 2.5 mA*
Input high	*2.0 volts, min, +5.5 volts absolute, max*
Input low	*0.8 volts, max, -0.5 volts absolute, min*
Power-up / reset state	*Input mode (high impedance)*
Interrupts	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable
Interrupt sources	Residual counter, end-of-channel-scan, AD-FIFO-not-empty, AD-FIFO-half-full

Counters

Table 3. Counter specifications

Parameter		Specification
Counter type		*82C54*
Configuration		*Two 82C54 devices. 3 down counters per 82C54, 16 bits each*
82C54A:	Counter 0 - ADC residual sample counter.	▪ Source: ADC Clock. ▪ Gate: Internal programmable source. ▪ Output: End-of-Acquisition interrupt.
	Counter 1 - ADC pacer lower divider	▪ Source: 10 MHz oscillator ▪ Gate: tied to counter 2 gate, programmable source. ▪ Output: chained to counter 2 clock.
	Counter 2 - ADC pacer upper divider	▪ Source: counter 1 output. ▪ Gate: Tied to counter 1 gate, programmable source. ▪ Output: ADC pacer clock (if software selected), available at user connector.
82C54B:	Counter 0 - pretrigger mode	▪ Source: ADC clock ▪ Gate: external trigger ▪ Output: End-of-Acquisition interrupt
	Counter 0 - user counter 4 (when in non-pretrigger mode)	▪ Source: User input at 100-pin connector (CLK4) or internal 10 MHz (software selectable) ▪ Gate: user input at 100-pin connector (GATE4) ▪ Output: available at 100-pin connector (OUT4)
	Counter 1 - user counter 5	▪ Source: user input at 100-pin connector (CLK5) ▪ Gate: user input at 100-pin connector (GATE5) ▪ Output: available at 100-pin connector (OUT5)
	Counter 2 - user counter 6	▪ Source: user input at 100-pin connector (CLK6) ▪ Gate: user input at 100-pin connector (GATE6) ▪ Output: available at 100-pin connector (OUT6)
Clock input frequency		*10 MHz max*
High pulse width (clock input)		*30 ns min*
Low pulse width (clock input)		*50 ns min*
Gate width high		*50 ns min*
Gate width low		*50 ns min*
Input low voltage		*0.8 V max*
Input high voltage		*2.0 V min*
Output low voltage		*0.4 V max*
Output high voltage		*3.0 V min*

Power consumption

Table 4. Power consumption specifications

Parameter	Specification
+5 V operating (A/D converting to FIFO)	0.8 A typical, 1.0 A max

Environmental

Table 5. Environmental specifications

Parameter	Specification
Operating temperature range	*0 to 70 °C*
Storage temperature range	*-40 to 100 °C*
Humidity	*0 to 90% non-condensing*

Main connector and pin out

Connector type	100-pin high density	
Compatible cable	C100FF-x, unshielded ribbon cable. x = length in feet	
Compatible accessory products (with C100FF-x cable)	ISO-RACK16/P ISO-DA02/P CIO-ERB24 (DADP-5037 adaptor required) CIO-SERB24 (DADP-5037 adaptor required) SSR-RACK24 (DADP-5037 adaptor required)	BNC-16SE BNC-16DI CIO-MINI50 (2 required) CIO-TERM100 (1 required) SCB-50 (1 required)

8-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 IN HI	52	FIRSTPORTA Bit 1
3	CH0 IN LO	53	FIRSTPORTA Bit 2
4	CH1 IN HI	54	FIRSTPORTA Bit 3
5	CH1 IN LO	55	FIRSTPORTA Bit 4
6	CH2 IN HI	56	FIRSTPORTA Bit 5
7	CH2 IN LO	57	FIRSTPORTA Bit 6
8	CH3 IN HI	58	FIRSTPORTA Bit 7
9	CH3 IN LO	59	FIRSTPORTB Bit 0
10	CH4 IN HI	60	FIRSTPORTB Bit 1
11	CH4 IN LO	61	FIRSTPORTB Bit 2
12	CH5 IN HI	62	FIRSTPORTB Bit 3
13	CH5 IN LO	63	FIRSTPORTB Bit 4
14	CH6 IN HI	64	FIRSTPORTB Bit 5
15	CH6 IN LO	65	FIRSTPORTB Bit 6
16	CH7 IN HI	66	FIRSTPORTB Bit 7
17	CH7 IN LO	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	CTR6 CLK
31	N/C	81	CTR6 GATE
32	N/C	82	CTR6 OUT
33	N/C	83	N/C
34	N/C	84	N/C
35	N/C	85	CTR5 CLK
36	N/C	86	CTR5 GATE
37	N/C	87	CTR5 OUT
38	N/C	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	N/C	93	N/C
44	N/C	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	N/C
47	N/C	97	N/C
48	PC +5V	98	N/C
49	N/C	99	N/C
50	GND	100	GND

16-channel single-ended mode pin out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 IN	52	FIRSTPORTA Bit 1
3	CH8 IN	53	FIRSTPORTA Bit 2
4	CH1 IN	54	FIRSTPORTA Bit 3
5	CH9 IN	55	FIRSTPORTA Bit 4
6	CH2 IN	56	FIRSTPORTA Bit 5
7	CH10 IN	57	FIRSTPORTA Bit 6
8	CH3 IN	58	FIRSTPORTA Bit 7
9	CH11 IN	59	FIRSTPORTB Bit 0
10	CH4 IN	60	FIRSTPORTB Bit 1
11	CH12 IN	61	FIRSTPORTB Bit 2
12	CH5 IN	62	FIRSTPORTB Bit 3
13	CH13 IN	63	FIRSTPORTB Bit 4
14	CH6 IN	64	FIRSTPORTB Bit 5
15	CH14 IN	65	FIRSTPORTB Bit 6
16	CH7 IN	66	FIRSTPORTB Bit 7
17	CH15 IN	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	CTR6 CLK
31	N/C	81	CTR6 GATE
32	N/C	82	CTR6 OUT
33	N/C	83	N/C
34	N/C	84	N/C
35	N/C	85	CTR5 CLK
36	N/C	86	CTR5 GATE
37	N/C	87	CTR5 OUT
38	N/C	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	N/C	93	N/C
44	N/C	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	N/C
47	N/C	97	N/C
48	PC +5V	98	N/C
49	N/C	99	N/C
50	GND	100	GND

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