

USB-DIO32HS-OEM

High-Speed Digital I/O

User's Guide

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About this User's Guide

What you will learn from this user's guide

This user's guide describes the Measurement Computing USB-DIO32HS-OEM data acquisition device and lists device specifications.

Conventions in this user's guide

For more information

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

bold text **Bold** text is used for the names of objects on a screen, such as buttons, text boxes, and check boxes.

italic text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase.

Where to find more information

Additional information about the USB-DIO32HS-OEM is available on our website at www.mccdaq.com. You can also contact Measurement Computing Corporation by phone, fax, or email with specific questions.

- Knowledgebase: kb.mccdaq.com
- Tech support form: www.mccdaq.com/support/support_form.aspx
- Email: techsupport@mccdaq.com
- Phone: 508-946-5100 and follow [the instructions for reaching Tech Support](#)

For international customers, contact your local distributor. Refer to the International Distributors section on our website at www.mccdaq.com/International.

Introducing the USB-DIO32HS-OEM

The USB-DIO32HS-OEM is a USB 2.0 high-speed synchronous digital I/O device that provides the following features:

- 32 bits of bidirectional TTL digital I/O
- Pattern detection and generation
- Input scan rate up to 8 MS/s
- Output update rate up to 8 MS/s
- Independent input and output scan clocks
- 24 mA source, 10 mA sink output current
- External trigger input
- Board-only form factor
- Header connectors for field wiring connections

The USB-DIO32HS-OEM is powered by the +5 volt USB supply from your computer; no external power is required.

Functional block diagram

USB-DIO32HS-OEM functions are illustrated in the block diagram shown here.

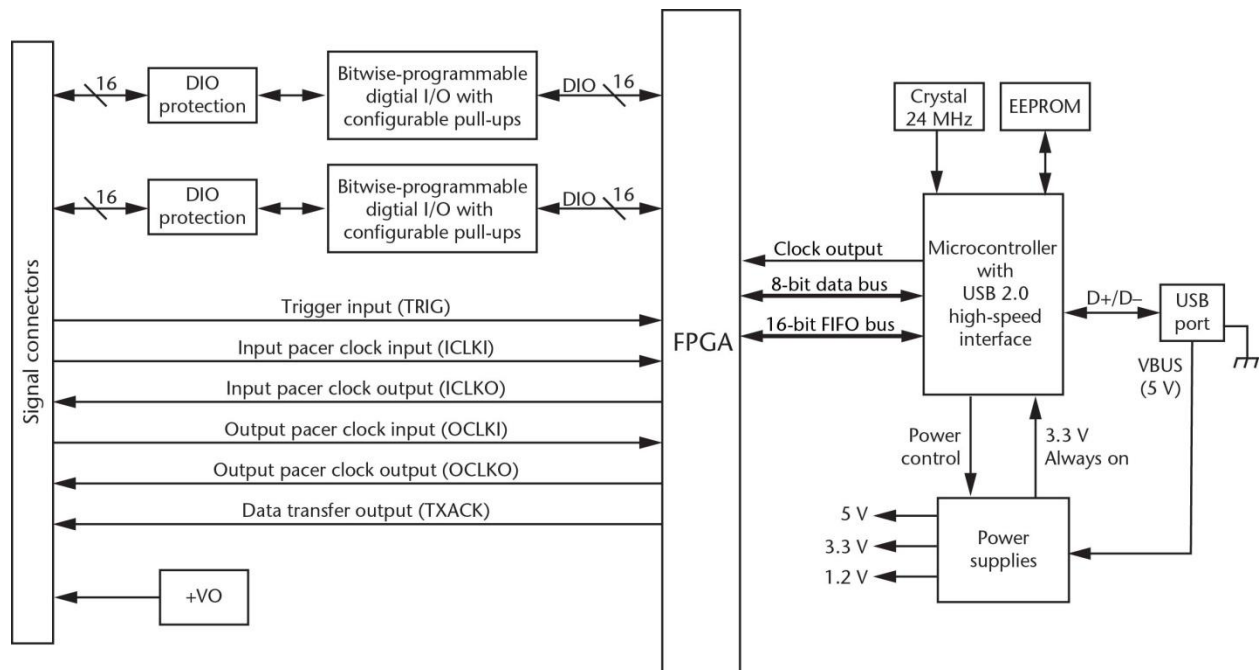


Figure 1. Functional block diagram

Installing the USB-DIO32HS-OEM

Unpacking

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the device from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

Contact us immediately if any components are missing or damaged.

Installing the software

Refer to the MCC DAQ Quick Start for instructions on installing the software on the MCC DAQ CD. Refer to the device product page on the Measurement Computing website for information about the included and optional software supported by the USB-DIO32HS-OEM.

Install the software before you install your device

The driver needed to run the USB-DIO32HS-OEM is installed with the software. Therefore, you need to install the software package you plan to use before you install the hardware.

Installing the hardware

To connect a USB-DIO32HS-OEM to your system, turn on your computer and connect a USB cable to an available USB port on the computer or to an external USB hub connected to the computer. Connect the other end of the USB cable to the USB connector on the device. No external power is required. A green **Status LED** turns on when power is applied.

When you connect the device for the first time, a **Found New Hardware** dialog opens when the operating system detects the device. The dialog closes after the device is installed.

Firmware updates

Your DAQ device contains firmware that can be updated in the field if required. Firmware is available for download at www.mccdaq.com/firmware.aspx. We recommend that you check this page periodically to see if an update to your device firmware is available.

Functional Details

External components

USB-DIO32HS-OEM has the following components, as shown in Figure 2:

- Header connectors (2)
- Pull-up/down jumpers (4)
- LED indicators (2)
- USB connector

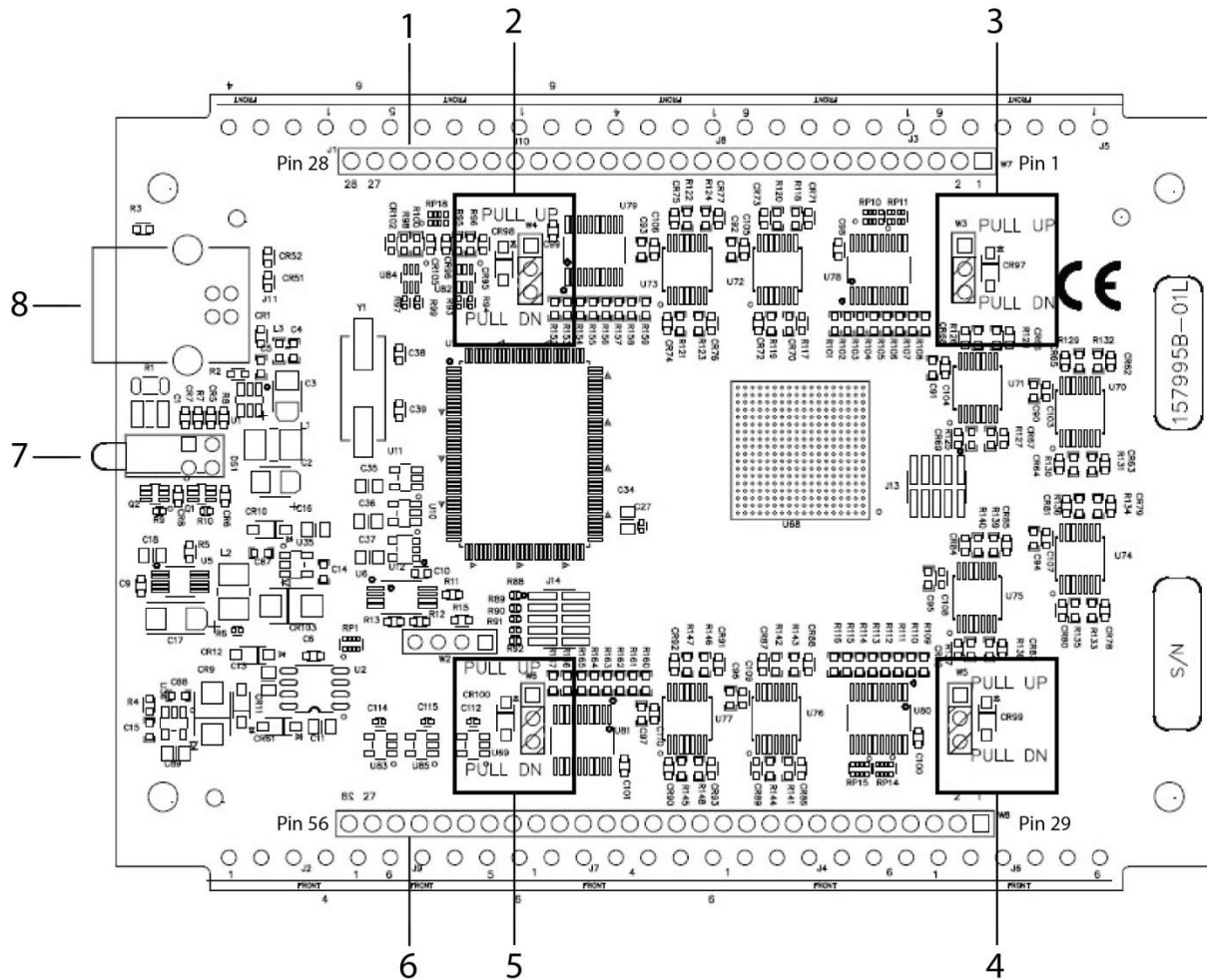


Figure 2. USB-DIO32HS-OEM components

- | | |
|---|--|
| 1 Header connector pin 1 to 28 (Port 0) | 5 Pull-up/down jumper W6 |
| 2 Pull-up/down jumper W4 | 6 Header connector pin 29 to 56 (Port 1) |
| 3 Pull-up/down jumper W3 | 7 LED indicators (2) |
| 4 Pull-up/down jumper W5 | 8 USB connector |

Header connectors

The header connectors provide the following connections:

- 32 digital I/O bits configured as two 16-bit ports (**P0D0** to **P1D15**)
- External input scan clock input (**ICLKI**) and output (**ICLKO**) for digital inputs
- External output scan clock input (**OCLKI**) and output (**OCLKO**) for digital outputs
- External trigger input (**TRIG**)
- Data transfer output (**TXACK**)
- Power output (**+VO**)
- Digital ground (**GND**)

The USB-DIO32HS-OEM pinout is shown below. Refer to Figure 2 on page 7

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	P0D0	Port 0 bit 0	29	P1D0	Port 1 bit 0
2	P0D1	Port 0 bit 1	30	P1D1	Port 1 bit 1
3	GND	Digital ground	31	GND	Digital ground
4	P0D2	Port 0 bit 2	32	P1D2	Port 1 bit 2
5	P0D3	Port 0 bit 3	33	P1D3	Port 1 bit 3
6	GND	Digital ground	34	GND	Digital ground
7	P0D4	Port 0 bit 4	35	P1D4	Port 1 bit 4
8	P0D5	Port 0 bit 5	36	P1D5	Port 1 bit 5
9	GND	Digital ground	37	GND	Digital ground
10	P0D6	Port 0 bit 6	38	P1D6	Port 1 bit 6
11	P0D7	Port 0 bit 7	39	P1D7	Port 1 bit 7
12	GND	Digital ground	40	GND	Digital ground
13	P0D8	Port 0 bit 8	41	P1D8	Port 1 bit 8
14	P0D9	Port 0 bit 9	42	P1D9	Port 1 bit 9
15	GND	Digital ground	43	GND	Digital ground
16	P0D10	Port 0 bit 10	44	P1D10	Port 1 bit 10
17	P0D11	Port 0 bit 11	45	P1D11	Port 1 bit 11
18	GND	Digital ground	46	GND	Digital ground
19	P0D12	Port 0 bit 12	47	P1D12	Port 1 bit 12
20	P0D13	Port 0 bit 13	48	P1D13	Port 1 bit 13
21	GND	Digital ground	49	GND	Digital ground
22	P0D14	Port 0 bit 14	50	P1D14	Port 1 bit 14
23	P0D15	Port 0 bit 15	51	P1D15	Port 1 bit 15
24	GND	Digital ground	52	GND	Digital ground
25	ICLKI	Input scan clock input	53	ICLKO	Input scan clock output
26	OCLKI	Output scan clock input	54	OCLKO	Output scan clock output
27	TRIG	External trigger input	55	+VO	User voltage output
28	RSVD	Reserved for future use	56	TXACK	Handshaking transfer output

Pull-up/down configuration

Unconnected inputs are pulled low to 0 V through 47 k Ω resistors via onboard jumpers **W3** to **W6**.

- W3 configures port 0 bit 0 to bit 7
- W4 configures port 0 bit 8 to bit 15
- W5 configures port 1 bit 0 to bit 7
- W6 configures port 1 bit 8 to bit 15

The pull-up/down voltage is common to all 47 k Ω resistors. Refer to Figure 2 on page 7 for the location of each jumper.

Each jumper is configured for pull-down by default (see Figure 3). Jumper pins 1 and 2 if you want to configure the inputs to pull-high (+5V).

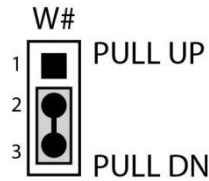


Figure 3. Pull-up/down jumper, default

For more information about digital signal connections

For general information about digital signal connections and digital I/O techniques, refer to the *Guide to DAQ Signal Connections* (available on our web site at www.mccdaq.com/signals/signals.pdf).

LED indicators

The USB-DIO32HS-OEM has two LED indicators that indicate the status of power and data. The LEDs are stacked one above the other.

- The **Status** LED (top) turns on when power is applied.
- The **Activity** LED (bottom) blinks when data is being transferred.

USB connector

The USB connector provides +5 V power and communication. No external power supply is required.

Signal connections

Digital I/O

The USB-DIO32HS-OEM provides 32 digital I/O bits that are configured as two ports of 16-bits each. You can connect up to 16 DIO lines to port 0 (**P0D0** through **D0D15**), and up to 16 DIO lines to port 1 (**P1D0** through **P1D15**). Each digital bit is individually configurable for input or output. Refer to [Digital operations](#) on page 10 for more information.

Clock I/O

You can pace input scanning operations using the onboard input scan clock or with an external signal connected to **ICKLI**. The input clock frequency is 8 MHz, maximum.

When the internal input clock paces operations, a duty cycle of 50% is maintained on **ICKKO**. When an external clock is used, the signal is output immediately after the external clock input is received.

Input pacer clock connections:

- **ICKLI**: accepts an external scan clock signal to pace the internal input scan.
- **ICKKO**: outputs the internal input scan clock. When externally clocked, this pin outputs a delayed version of the **ICKLI** signal. The delay is no more than 83.33 ns, and is due to the time required for the signal to propagate from the external clock to the device's FPGA before it is output.

You can pace the output pattern generation using the onboard output scan clock or with an external signal connected to **OCKLI**. The output clock frequency is 8 MHz, maximum.

Output pacer clock connections:

- **OCKLI**: accepts an external scan clock signal to pace the output scan.
- **OCKKO**: outputs the internal output scan clock. When externally clocked, this pin outputs a delayed version of the **OCKLI** signal. The delay is no more than 83.33 ns, and is due to the time required for the signal to propagate from the external clock to the device's FPGA before it is output.

Trigger input

The **TRIG** terminal is an external digital trigger input that can be used to trigger digital input or output scans.

Data transfer output

The **TXACK** pin is a timing output that may be used when transferring data to an external peripheral device or to a second USB-DIO32HS-OEM. Refer to the [Digital output scanning](#) section below for more information.

User voltage power output

The **+VO** terminal can output up to 10 mA maximum. You can use this terminal to supply power to external devices or circuitry.

Caution! The **+VO** terminal is an output. Do not connect to an external power supply or you may damage the device and possibly the computer.

Ground

The digital ground (**GND**) pins provide a common ground for all I/O signals and the power terminal.

Digital operations

When performing software polling operations, the port can contain any combination of input or output bits. When performing hardware-paced output scans, all bits in the port must be set for output. For input scans, however, any bits in the port that are configured for output are ignored. Since each port is configured independently, both software polling and hardware scanning operations can be performed at the same time.

The digital I/O terminals can detect the state of any TTL-level input. Refer to the schematic shown in Figure 4.

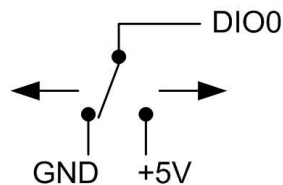


Figure 4. Schematic showing switch detection by digital channel DIO0

When set to the +5 V input, DIO0 reads *TRUE* (1). When switched to GND, DIO0 reads *FALSE* (0).

Digital output scanning

Digital outputs can source 24 mA and sink 10 mA.

Either port can output a 16-bit digital pattern. The pattern is updated at a rate up to 8 MS/s, and clocked using the output scan clock.

Use both ports to output a 32-bit digital pattern. Data from one port is read and stored in the FIFO buffer until the second port is read. Both ports are output simultaneously to the pins on the rising edge of the next pacer clock signal.

The USB-DIO32HS-OEM utilizes a delay between the output scan clock and the **TXACK** pin output. When each data value of an output scan is output, the **TXACK** pin is updated after a lag of 83.33 nS. This delay allows an external device that is accepting the data to know that the data is stable at that point, and ensures a coherent data transfer between devices.

When transferring data to a second (slave) USB-DIO32HS-OEM, the input scan clock on the slave device is paced by the **TXACK** pin on the master device to ensure that the output data of the master is valid when acquired by the slave.

Triggering

The USB-DIO32HS-OEM supports digital and pattern triggering to start a scan.

Digital triggering

The **TRIG** pin is used for external TTL-level triggering, and can be used to trigger input or output scans. Trigger latency is less than 1 μ s. The trigger mode is software-selectable for edge or level sensitive, and high or low logic. The default setting at power up is edge sensitive, rising edge. You can set up a repetitive trigger mode with software. When retrigger mode is enabled the trigger is automatically re-armed after it is activated.

Pattern triggering

You can start an input or output scan using a digital pattern trigger. Either port 0 (default) or port 1 can be used for pattern triggering. The pattern represents the state of up to 16 bits on the port.

You specify the pattern and the trigger type with software. Supported trigger types are Above Pattern, Below Pattern, Equal Pattern, and Not Equal Pattern. The scan begins when the trigger conditions are met.

The base clock is fixed at 96 MHz (10.416 ns). The trigger pattern must be held for three base clock cycles (31.25 ns) to ensure that it is properly detected. The trigger latency is 1 scan clock period + 8 base clock cycles (83.328 ns).

Signals after the trigger are ignored by the trigger circuit. You can increase the clock frequency up to 8 MHz to change how fast a pattern is detected.

Mask option

Use a bitmask to specify which bits to include or exclude from the pattern to detect. To include a bit in the pattern, sets its value to 1. To exclude a bit from the pattern, sets its value to 0. Refer to the pattern and mask values shown in Figure 5 and Figure 6.

In Figure 5 all mask bits are set to 1, so all of the bits are included in the pattern to detect.

	Bit 15	Bit 8	Bit 4	Bit 0
Pattern	1101	0000	1111	1010
Mask	1111	1111	1111	1111 (AND)
	1101	0000	1111	1010

Figure 5. Trigger mask with all bits included

In Figure 6 all mask bits are excluded except bits 4 to 7. The result of this operation is that only bits 4 through 7 are included in the pattern to detect.

	Bit 15	Bit 8	Bit 4	Bit 0
Pattern	1101	0000	1111	1010
Mask	0000	0000	1111	0000 (AND)
	0000	0000	1111	0000

Figure 6. Trigger mask with some bits excluded

Mechanical drawing

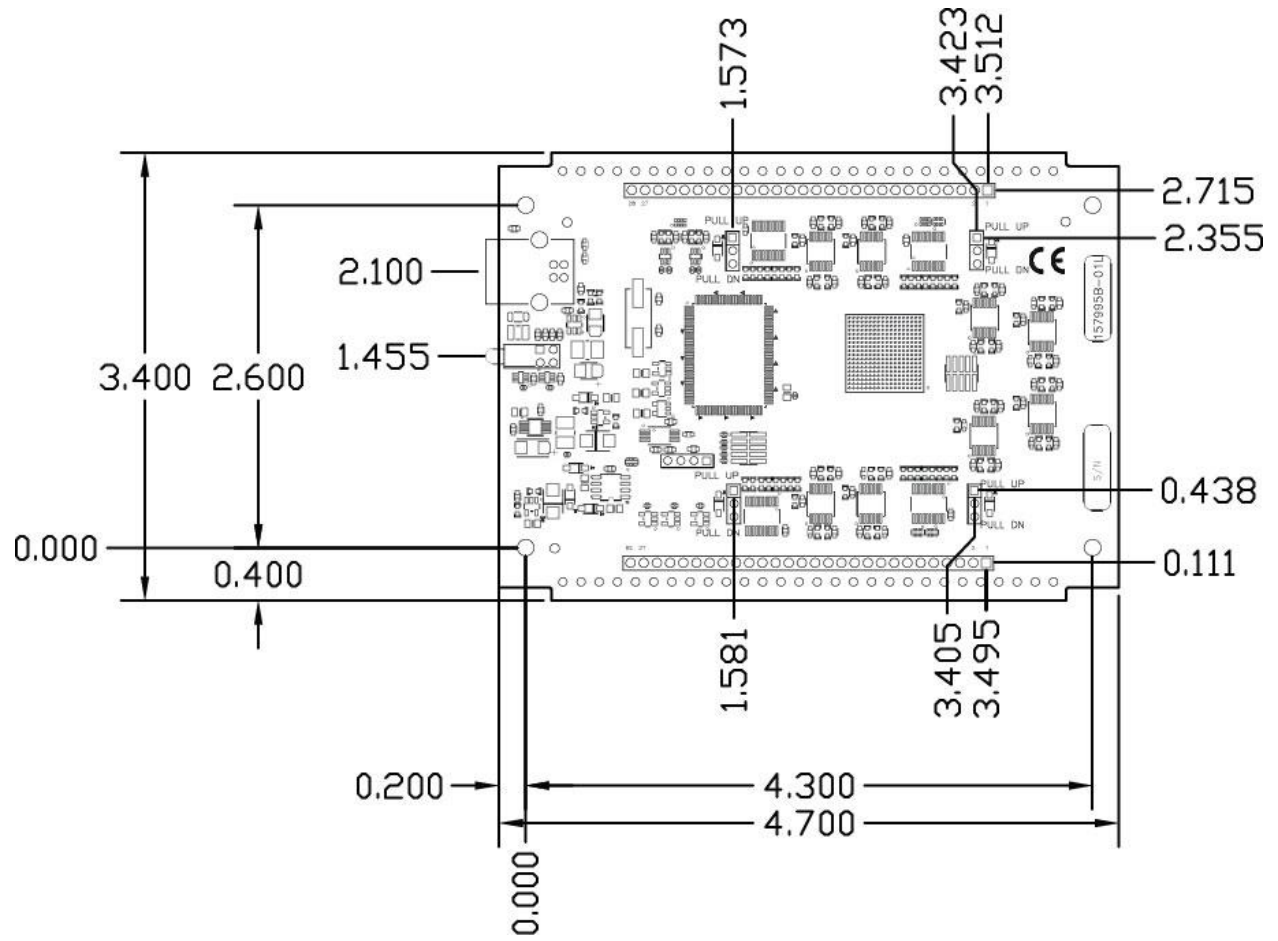


Figure 7. USB-DIO32HS-OEM circuit board dimensions

Specifications

All specifications are subject to change without notice.

Typical for 25°C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Digital input/output

Table 1. Digital I/O specifications

Parameter	Specification
Digital type	TTL
Number of I/O	32 (2 ports of 16 bits)
Configuration	Bit-configurable as input (power on default) or output
Pull-up configuration	Each port has two 47 k Ω resistors configurable as a pull-up or pull-down (default) with an internal jumper. Each jumper configures 8 digital bits. <ul style="list-style-type: none"> ■ Jumper W3 configures port 0 bit 0 to bit 7 ■ Jumper W4 configures port 0 bit 8 to bit 15 ■ Jumper W5 configures port 1 bit 0 to bit 7 ■ Jumper W6 configures port 1 bit 8 to bit 15
Digital I/O transfer rate (system-paced, asynchronous)	33 to 8000 port reads/writes or single bit reads/writes per second typical, system dependent.
Digital I/O transfer rate (synchronous)	0.022 Hz to 8 MHz, based on the internal clock speed of 96 MHz
Digital input pacing	Onboard clock, external input scan clock (ICLKI)
Digital input trigger source	External single channel digital trigger (TRIG) or Pattern Detection
Digital output pacing	Onboard clock, external output scan clock (OCLKI)
Digital output trigger source	External single channel digital trigger (TRIG) or Pattern Detection
Input high voltage	2.0 V min 5.0 V absolute max
Input low voltage	0.8 V max 0 V recommended min
Output high voltage	4.4 V min (IOH = -50 μ A) 2.96 V min (IOH = -24 mA)
Output low voltage	0.1 V max (IOL = 50 μ A) 0.77 V max (IOL = 10 mA)
Output current	24 mA source, 10 mA sink max per pin, constrained to 384 mA across all output pins (digital outputs, pacer clock outputs, and +VO)

External trigger

Table 2. Digital trigger specifications

Parameter	Specification
Trigger source	External digital; TRIG terminal
Trigger mode	Software-selectable for edge or level sensitive, rising or falling edge, high or low level.
Retrigger mode	Trigger is rearmed after each trigger event
Trigger latency	100 ns max
Trigger pulse width	100 ns min
Input type	Schmitt trigger, 47 k Ω pull-down to ground with 33 Ω in series

Parameter	Specification
Schmitt trigger hysteresis	0.76 V typ 0.4 V min 1.2 V max
Input high voltage threshold	1.74 V typ 1.3 V min 2.2 V max
Input high voltage limit	5.5 V absolute max
Input low voltage threshold	0.98 V typ 0.6 V min 1.5 V max
Input low voltage limit	-0.5 V absolute min 0 V recommended min

Pattern trigger

Table 3. Pattern trigger specifications

Parameter	Specification
Trigger source	Port 0 or Port 1
Trigger types	Above pattern, Below pattern, Equal pattern, or Not equal pattern
Trigger stability	Digital port must be stable for 31.25 ns to be recognized as a pattern
Trigger bit width	Up to 16, adjustable through bitmask
Trigger latency	Up to 1 scan period

Clock input/output

Table 4. Clock I/O specifications

Parameter	Specification
Terminal names	ICLKI, ICLKO, OCLKI, OCLKO
Terminal type	ICLKI: Input scan clock input, active on rising edge ICLKO: Input scan clock output, power on default is 0V, active on rising edge OCLKI: Output scan clock input, active on rising edge OCLKO: Output scan clock output, power on default is 0V, active on rising edge
Input clock frequency	8 MHz, max
Input clock pulse width	10.417 ns min
Input type	Schmitt trigger, 47 k Ω pull-down to ground with 33 Ω in series
Input Schmitt trigger hysteresis	0.76 V typ 0.4 V min 1.2 V max
Input high voltage threshold	1.74 V typ 1.3 V min 2.2 V max
Input high voltage limit	5.5 V absolute max
Input low voltage threshold	0.98 V typ 0.6 V min 1.5 V max
Input low voltage limit	-0.5 V absolute min 0 V recommended min
Output clock frequency	8 MHz, max
Output clock pulse width	Minimum 62.5 ns at 8 MHz, but varies according to the sample rate; always maintains a 50% duty cycle when using the internal clock. When using the external clock, it follows the external clock input.

Output high voltage	4.4 V min (IOH = -50 μ A) 2.96 V min (IOH = -24 mA)
Output low voltage	0.1 V max (IOL = 50 μ A) 0.77 V max (IOL = 10 mA)
Output current	24 mA source, 10 mA sink max per pin, constrained to 384 mA across all output pins (digital outputs, pacer clock outputs, and +VO)
Handshaking	The TXACK output will have an 83.33 ns delay from the OCLKO signal to ensure coherent data transfers between devices.

Memory

Table 5. Memory specifications

Parameter	Specification
FIFO	8 KS
Non-volatile EEPROM	32 KB (10 KB firmware storage, 22 KB user data)

Power

Table 6. Power specifications

Parameter	Condition	Specification
Supply current, USB source	During enumeration	< 100 mA
	After USB enumeration	< 500 mA
+VO voltage output range	After USB enumeration	5 V, \pm 5%
+VO output current	After USB enumeration	24 mA max per pin, constrained to 384 mA across all output pins (digital outputs, pacer clock outputs, and +VO)

USB

Table 7. USB specifications

Parameter	Specification
USB device type	USB 2.0 (high-speed)
Device compatibility	USB 1.1, USB 2.0, USB 3.0
USB cable type	A-B cable, UL type AWM 2725 or equivalent. (Min 24 AWG VBUS/GND, min 28 AWG D+/D-)
USB cable length	3 m (9.84 ft) max

Environmental

Table 8. Environmental specifications

Parameter	Specification
Operating temperature range	0 $^{\circ}$ C to 50 $^{\circ}$ C
Storage temperature range	-40 $^{\circ}$ C to 70 $^{\circ}$ C
Humidity	0% to 90% non-condensing

Mechanical

Table 9. Mechanical specifications

Parameter	Specification
Dimensions (L \times W \times H)	119.38 \times 86.36 \times 15.24 mm (4.70 \times 3.40 \times 0.60 in.)

Header connector

Table 10. Header connector specifications

Parameter	Specification
Connector type	Two 1 × 28 pin 0.1 in. pitch headers

Header pinout

Table 11. Header pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	P0D0	Port 0 bit 0	29	P1D0	Port 1 bit 0
2	P0D1	Port 0 bit 1	30	P1D1	Port 1 bit 1
3	GND	Digital ground	31	GND	Digital ground
4	P0D2	Port 0 bit 2	32	P1D2	Port 1 bit 2
5	P0D3	Port 0 bit 3	33	P1D3	Port 1 bit 3
6	GND	Digital ground	34	GND	Digital ground
7	P0D4	Port 0 bit 4	35	P1D4	Port 1 bit 4
8	P0D5	Port 0 bit 5	36	P1D5	Port 1 bit 5
9	GND	Digital ground	37	GND	Digital ground
10	P0D6	Port 0 bit 6	38	P1D6	Port 1 bit 6
11	P0D7	Port 0 bit 7	39	P1D7	Port 1 bit 7
12	GND	Digital ground	40	GND	Digital ground
13	P0D8	Port 0 bit 8	41	P1D8	Port 1 bit 8
14	P0D9	Port 0 bit 9	42	P1D9	Port 1 bit 9
15	GND	Digital ground	43	GND	Digital ground
16	P0D10	Port 0 bit 10	44	P1D10	Port 1 bit 10
17	P0D11	Port 0 bit 11	45	P1D11	Port 1 bit 11
18	GND	Digital ground	46	GND	Digital ground
19	P0D12	Port 0 bit 12	47	P1D12	Port 1 bit 12
20	P0D13	Port 0 bit 13	48	P1D13	Port 1 bit 13
21	GND	Digital ground	49	GND	Digital ground
22	P0D14	Port 0 bit 14	50	P1D14	Port 1 bit 14
23	P0D15	Port 0 bit 15	51	P1D15	Port 1 bit 15
24	GND	Digital ground	52	GND	Digital ground
25	ICLKI	Input scan clock input	53	ICLKO	Input scan clock output
26	OCLKI	Output scan clock input	54	OCLKO	Output scan clock output
27	TRIG	External trigger input	55	+VO	User voltage output
28	RSVD	Reserved for future use	56	TXACK	Data transfer output

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