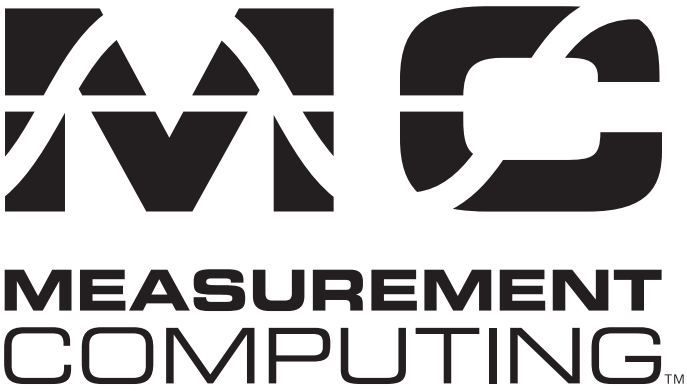
SPECIFICATIONS

CIO-PDMA16
CIO-PDMA32

High Speed Digital I/O



Revision 5, October, 2000

Typical for 25°C unless otherwise specified.

Power Consumption

+5VDC	
CIO-PDMA16	850 mA typical, 1.0 A maximum
CIO-PDMA32	900 mA typical, 1.1 A maximum

Digital Input / Output

Digital Type - Auxiliary	
Configuration	Output
Number of channels	3
CIO-PDMA16	74LS273
Output High	2.7 volts minimum @ –0.4 mA
Output Low	0.5 volts maximum@ 8 mA
Input High	2.0 volts minimum, 7 volts absolute maximum
Input Low	0.8 volts maximum, –0.5 volts absolute minimum
CIO-PDMA32	74LS125
Output High	2.4 volts minimum @ –2.6 mA
Output Low	0.5 volts maximum @ 24 mA
Input High	2.0 volts minimum, 7 volts absolute maximum
Input Low	0.8 volts maximum, –0.5 volts absolute minimum
Digital Type Ports A & B	
CIO-PDMA16	
Output	74LS374
Input	74LS244
CIO-PDMA32	74LS245
Number of channels	16 I/O
Output High	2.4 volts minimum @ –2.6 mA
Output Low	0.5 volts maximum @ 24 mA
Input High	2.0 volts minimum, 7 volts absolute maximum
Input Low	0.8 volts maximum, –0.5 volts absolute minimum
Power-up / Reset State	Input mode (high impedance)
Digital Pacing	Programmable: internal counter, external source (Transfer Req In) or software polled
Data Transfer	
CIO-PDMA16	Interrupt, DMA or software polled
CIO-PDMA32	From 512 sample FIFO via REPINSW, interrupt, DMA or software polled
DMA	
CIO-PDMA16	Channel 1 or 3, software-selectable
CIO-PDMA32	Channel 5, 6, or 7,software-selectable
Throughput	
CIO-PDMA16	250 KBytes, 125 KWords / sec synchronous
CIO-PDMA32 (DMA)	400 KBytes, 200 KWords / sec synchronous
CIO-PDMA32 (REPIN/OUTS)	1500 KBytes, 750 KWords / sec synchronous
Interrupts	
CIO-PDMA16	Levels 2 to 7, software-selectable
CIO-PDMA32	Levels 2 to 15, software-selectable
Interrupt enable	Programmable
Interrupt sources	External (Int In, positive or negative edge software-selectable), DMA terminal count, Counter / Timer terminal count, software-selectable

Counter section

Counter type

CIO-PDMA16	82C54
CIO-PDMA32	82C54 emulator

Configuration 3 down-counters per 82C54, 16 bits each

Counter 0 - Internal pacer, lower divider (mode 2 only for CIO-PDMA32)

Source:	10 MHz oscillator
Gate:	Wired to counter 1 gate, pulled high through 10k resistor. Available at user connector (Timer Gate In)
Output:	Wired to counter 1 and counter 2 clock inputs

Counter 1 - Internal pacer, upper divider (mode 2 only for CIO-PDMA32)

Source:	Counter 0 output
Gate:	Wired to counter 0 gate, pulled high through 10k resistor. Available at user connector (Timer Gate In)
Output:	Wired through inverter to user connector (Timer Out). Program-selectable as DMA Request source (internal pacer)

Counter 2 - CIO-PDMA16 (user counter 3)

Source:	Counter 0 output.
Gate:	Pulled high through 10k resistor
Output:	Not connected

Counter 2 - CIO-PDMA32 Used internally for REPINS / REPOUTS modes (configured as mode 2 8254 emulator)

Source:	Internal use
Gate:	Internal use
Output:	Internal use

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Crystal oscillator

Frequency	10 MHz
Frequency accuracy	100 ppm

Environmental

Operating temperature range	0 to 60°C
Storage temperature range	–40 to 100°C
Humidity	0 to 95% non-condensing

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