

# DAC488HR/4

## 16-bit D/A Converter with Digital I/O & IEEE 488

### Features

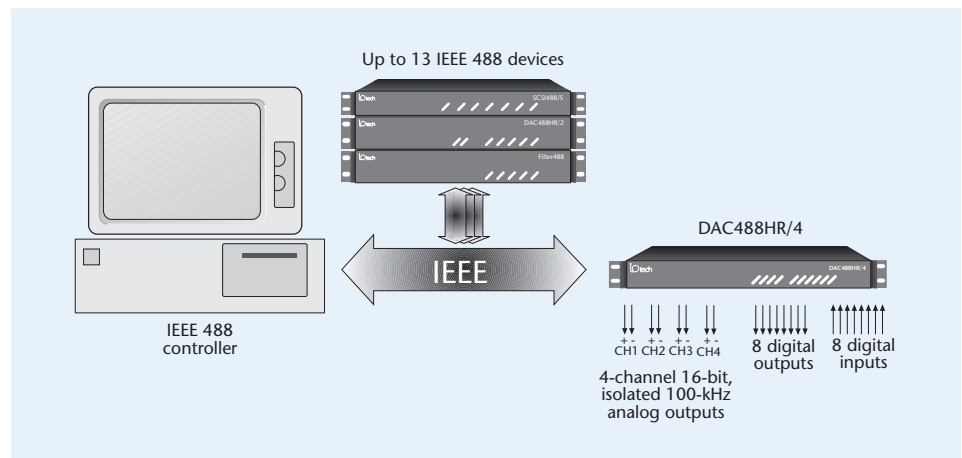
- Four isolated 16-bit outputs
- 100 kHz/channel update rate
- 480 Ksamples/channel max buffer
- $\pm 1$ ,  $\pm 2$ ,  $\pm 5$ , and  $\pm 10$  VFS programmable unipolar and bipolar output ranges
- One-shot, step, burst, waveform, and continuous output modes
- GET, external TTL, IEEE command, and time event trigger sources
- ASCII, binary, integer decimal, and hexadecimal data formats
- Standard sine, square, and triangle waveform generation
- 500 VDC channel-to-channel isolation
- Eight digital inputs and eight digital outputs
- 100 mA high-current outputs

The DAC488HR/4 is an IEEE 488 programmable 16-bit D/A converter. It is configured with four output channels which are optically isolated from each other and from IEEE 488 common by up to 500 VDC. Each channel is independently programmable for 1, 2, 5, or 10 VFS unipolar or bipolar output, specified as either bits or volts in ASCII, integer, hexadecimal, or binary format. Multiple output modes, multiple clock and trigger sources, and buffer management enable the DAC488HR/4 to function as a precision voltage source, a function generator, or an arbitrary waveform generator.

Waveforms captured by IOtech's 16-bit, 100 kHz ADC488/A Series digitizers can be edited and transferred to the DAC488HR/4 for output. The ADC488/A Series and DAC488HR/4 in combination form a powerful waveform I/O system. Typical applications include transducer simulation, disk-drive testing, vibration analysis, and materials testing.



*The versatile DAC488HR/4 functions as a voltage source, function generator, and an arbitrary waveform generator*



### Trigger Modes

The DAC488HR/4's five trigger modes support a wide variety of applications.

**Bus Control Mode.** Each port is programmed to output a specified value under direct control from the IEEE 488 bus. This mode is useful for maintaining an initial value until a specified condition occurs.

**Step Mode.** When a specified trigger is detected, a value is output from the buffer, and the DAC488HR/4 is automatically re-armed until the specified buffer count is reached. The last specified buffer value is held as the output.

**Burst Mode.** Functionally identical to step mode, except that waveforms rather than single values are output.

**Waveform Mode.** Based on recognition of a trigger, the waveform buffer is output for a specified number of cycles.

**Continuous Mode.** Data is continuously input from the IEEE 488 bus and output to an analog channel at rates up to 200 Kbytes/s upon the detection of a specified trigger. This mode is ideally suited for audio, speech, and other applications that require long duration waveforms.

# DAC488HR/4

## General Information

### DAC488HR/4 Design

Four independent analog output modules are optically isolated from the IEEE 488 bus, digital circuitry, earth ground, and chassis common by up to 500 VDC. Each module consists of a microcontroller and expandable data buffer. A common update clock is shared by all ports, ensuring synchronization. Four internal clock sources are available to meet a wide variety of applications including CD and DAT testing. An external clock source (up to 10 MHz) allows synchronization to an external frequency reference and can be used to synchronize the DAC488HR/4 to the ADC488/A Series digitizers for stimulus/response applications.

### Multiple Trigger Sources

All DAC488HR/4 ports share a common trigger source, ensuring multi-channel synchronization for applications with critical time and phase relationships. Trigger sources for the DAC488HR/4 include trigger command, IEEE 488 Group Execute Trigger (GET), and external TTL (rising or falling edge) signal input. Triggers can also be initiated on periodic intervals from 2 ms to 65,535 ms, specified in 1 ms increments. The DAC488HR/4 provides a delayed TTL-level trigger output for stimulus/response applications in which the device under test (DUT) must attain a steady state prior to measurement. This function allows users to specify a time delay, in update clock counts from 1 to 65,535, between the DAC488HR/4's output and the trigger signal's output.

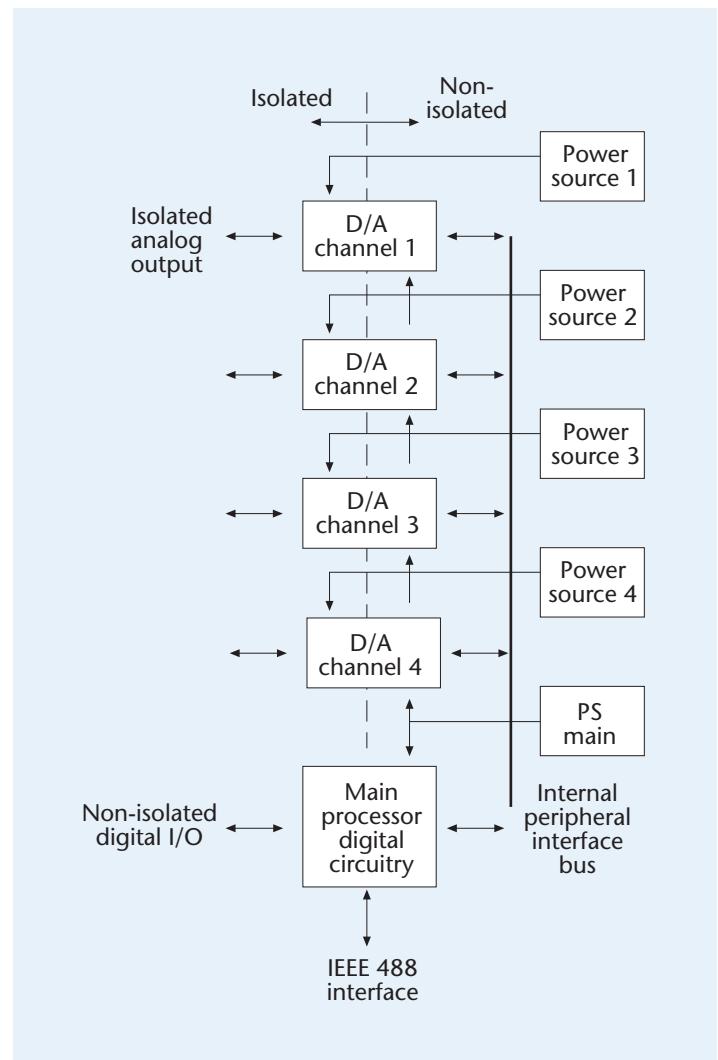
### Multiple Clock Sources

The DAC488HR/4 features four internal clock sources and accommodates an external clock source (up to 10 MHz) for updating the output ports. A 16-bit counter is used to provide update rates to meet application requirements. For example, the 200 kHz clock and the 5 MHz clock can be divided down to any rate between 3 Hz and 100 kHz for general purpose applications; the 5.6448 MHz clock can simulate 44.1 kHz audio CD signals; and the 6.144 MHz clock can simulate 48 kHz audio DAT signals. For synchronizing external circuitry to DAC488HR/4 output, an update clock signal is also provided.

### Buffer Management

The DAC488HR/4's step, burst, waveform, and continuous trigger output modes can be used with flexible buffer management functions to output stepped voltages, any one of five standard waveforms, or user-defined arbitrary waveforms. Waveforms are loaded from the IEEE 488 bus into the DAC488HR/4's resident 8 Ksample buffer at rates up to 500 Kbytes/s.

To output standard predefined sine, square, and triangle waveforms, the user specifies the starting memory location, number of samples, max/min values, duty cycle, and the number of times the cycle is to be repeated or "looped." The "looping" function outputs specified buffer segments up to the full available buffered size for repetition up to 65,535 times. This conserves memory space by allowing long periodic waveforms to be defined in



Each DAC488HR/4 output port features a separate microprocessor and buffer memory for independent waveform management

a single cycle. Additionally, for applications that exceed the DAC488HR/4's internal buffer capacity, waveforms can be output continuously from an IEEE 488 controller at up to 200 Kbytes/s via the IEEE 488 bus.

### Nonvolatile Storage

The DAC488HR/4 uses resident nonvolatile random access memory (NVRAM) to store the calibration constants determined during digital calibration, and to store its power-up default configuration.

# DAC488HR/4

## General Information



Functional Requirement	Waveform(s)	Typical Application
Continuously output a standard wave function under program control		Standard function generator outputs for general purpose applications
Output a series of voltage values based on TTL triggers		Sequenced V out for controlling power supplies or other analog programmable instruments
Initiate a trigger delay from 1 to 65,535 update clock pulses		Allows a device under test (DUT) to attain a steady state prior to measurement
Synchronously output multiple waveforms under program control		Ideal for stimulus/response applications with critical time and phase relationships
Output a standard waveform acquired by the ADC488/A Series digitizer		Ideal for simulating complex signals such as EKGs and contact bounce
Continuously output a large arbitrary waveform from the IEEE 488 bus at up to 200 Kbytes/s		For audio system testing, speech research, and other tests requiring long-time waveform generation

### Stimulus/Response System Multi-DAC488HR/4 Synchronization

When configured with an ADC488/A Series A/D converter, the DAC488HR/4 is well-suited for stimulus/response testing. For synchronous operation in which acquisition must begin simultaneously with the stimulus output, the DAC488HR/4's TTL trigger output is connected directly with the ADC488/A's TTL trigger input; for non-synchronous operation in which acquisition must begin at a specified time after the stimulus output, the DAC488HR/4's trigger output can be "delayed" up to 65,535 update clock counts.

Multiple DAC488HR/4s can be configured in master/slave mode to synchronously output data either from their internal buffers, or continuously from the IEEE 488 bus. When daisy-chained together the number of DAC488HR/4s in a system is limited only by the number of available IEEE 488 addresses, and the trigger "latency" between each unit is 60 ns\*. For applications that require non-additive trigger latencies, the DAC488HR/4s can be configured in parallel, limiting total system trigger latency to 60 ns.

\* A system with one master and three slave units will have a total system trigger latency of 180 ns

# DAC488HR/4

## Specifications & Ordering Information



### Specifications

#### Analog Output

**Number of Channels:** 4

**DC Output Voltage/Resolution**

1V Range:  $\pm 1V$ , 30.5  $\mu V$ /bit

2V Range:  $\pm 2V$ , 61  $\mu V$ /bit

5V Range:  $\pm 5V$ , 152  $\mu V$ /bit

10V Range:  $\pm 10V$ , 305  $\mu V$ /bit

**DC Output Current:**  $\pm 10$  mA max

**Accuracy (25  $\pm 5$  °C)**

$\pm 0.025\%$  of range

**Polarity:** Unipolar or bipolar (software selectable)

**Output Impedance:** 10 Ohm

**Zero Offset:** 50 to 500  $\mu V$

**Linearity:** 0.005%

**Differential Linearity:** 0.001%

**Update Rate:** 100 Ksamples/s (max per channel); all signals from the data buffer are 100 Ksamples/s max; any single channel from the IEEE 488 bus to output is 100 Ksamples/s max; any two channels from the IEEE 488 bus to output are 50 Ksamples/s max; any two channels from the IEEE 488 bus to multiple DAC488HR/4's are 20 Ksample/s

**Settling Time:** 6  $\mu s$  to 0.003% FSR

**Temperature Coefficient:** ( $\pm 0.002\% \pm 100 \mu V$ )/°C; 0 to 20 °C, 20 to 30 °C, and 30 to 50 °C

**Channel-to-Channel Isolation:** 500V max

**Channel-to-Digital Common and Chassis Isolation:** 500V max

**Connectors:** DB9 (female) per channel; mating connector supplied

#### Digital I/O

**Digital Inputs:** 8 TTL-level compatible, external TTL trigger, external TTL clock input

**Digital Outputs:** 8 TTL-level compatible, also configurable as open collector with 100 mA drive, and delayed trigger output signal, update clock output.

**Connectors:** DB15 (female) per input and output port; mating connector supplied

#### IEEE 488 Specifications

**Interface Subsets:** SH1, AH1, T6, TE6, L4, LE4, SR1, PP0, RL0, DC1, DT2, C0, and E2

**Connector:** Standard IEEE 488 connector with metric studs

#### Data Storage and Output

**Data Buffer:** 8 Ksamples standard (per channel); 480 Ksample option (per channel)

**Data Format:** ASCII, integer decimal, hexadecimal, and binary

**Output Modes:** Direct, step, burst, waveform, and continuous

**Trigger Sources:** GET, periodic time interval, external (TTL-level), and command

**Trigger Latency:** Daisy-chain mode; 60 ns (additive per unit) Parallel mode; 60 ns (non-additive system maximum)

#### General

**Power:** 90 to 125 or 210 to 250 VAC, 50/60 Hz; 20 VA max

**Environment:** 0 to 50 °C; 0 to 95% RH, non-condensing

**Controls:** Power switch, external dip switch for IEEE address

**Dimensions:** 425 mm W x 305 mm D x 45 mm H (16.75" x 12" x 1.75")

**Weight:** 3.6 kg (7.9 lbs)

**Supplied Accessories:** Analog output connector, digital I/O port connector

### Ordering Information

#### Description

Isolated 4-channel converter with 8 Ksample memory per channel; includes analog output connector; digital I/O port connector; and rack-mount kit

**Part No.**

DAC488HR/4

#### Accessories & Cables

Shielded IEEE 488 cable, 6 ft.

CA-7-3