

USB-CTR04

High-Speed Counter/Timer

User's Guide

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About this User's Guide

What you will learn from this user's guide

This user's guide describes the Measurement Computing USB-CTR04 data acquisition device and lists device specifications.

Conventions in this user's guide

For more information

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

bold text **Bold** text is used for the names of objects on a screen, such as buttons, text boxes, and check boxes.

italic text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase.

Where to find more information

Additional information about USB-CTR04 hardware is available on our website at www.mccdaq.com. You can also contact Measurement Computing Corporation with specific questions.

- Knowledgebase: kb.mccdaq.com
- Tech support form: www.mccdaq.com/support/support_form.aspx
- Email: techsupport@mccdaq.com
- Phone: 508-946-5100 and follow [the instructions for reaching Tech Support](#)

For international customers, contact your local distributor. Refer to the International Distributors section on our website at www.mccdaq.com/International.

Introducing the USB-CTR04

The USB-CTR04 is a USB 2.0 high-speed data acquisition device that provides the following features:

- Four counter I/O
 - High-speed pulse counter for general counting applications; multiple counting modes supported
 - 48 MHz, programmable resolution up to 64-bits
 - An aggregate scan rate of 8 MB/s
- Four PWM timers with count, period, delay, and pulse-width registers
- Eight individually-configurable digital I/O channels
- External clock input and internal clock output
- External digital trigger; software-selectable for edge or level sensitive, rising or falling edge, high or low level

The USB-CTR04 is a USB 2.0 high speed device that is compatible with USB 3.0 ports. The device is also compatible with USB 1.1 ports, but use with this older hardware is not recommended due to longer initialization times that can occur when the USB-CTR04 is connected through USB 1.1 ports or hubs.

I/O connections are made to two banks of screw terminals. The USB-CTR04 is powered by the 5 volt USB supply from your computer.

Functional block diagram

Device functions are illustrated in the block diagram shown here.

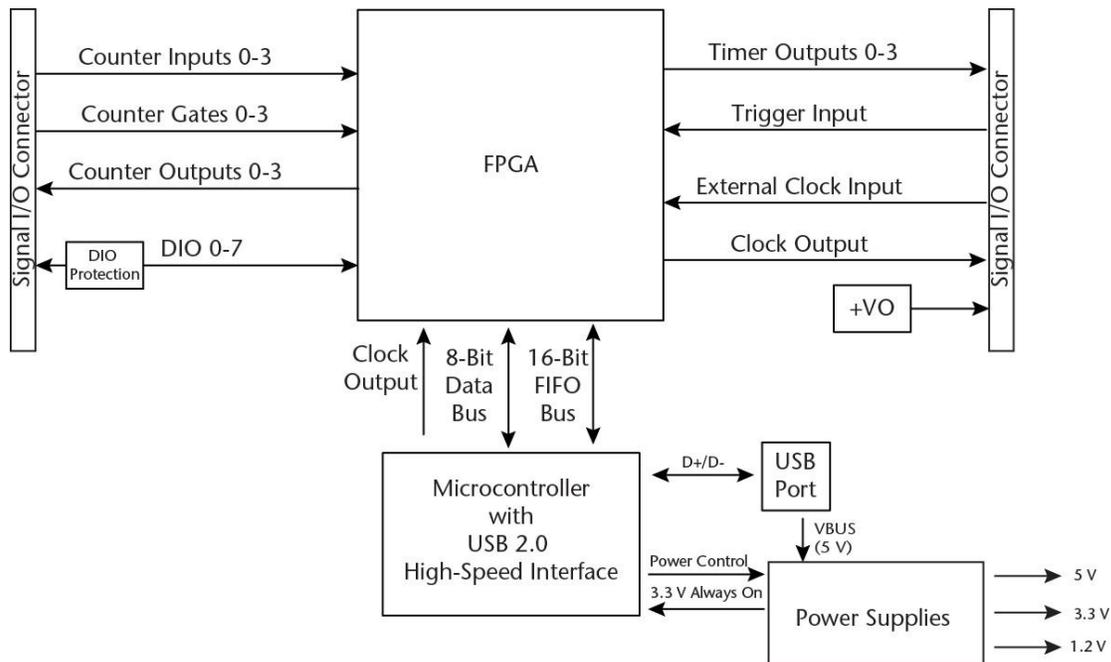


Figure 1. USB-CTR04 functional block diagram

Installing the USB-CTR04

Unpacking

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the device from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

Contact us immediately if any components are missing or damaged.

Installing the software

Refer to the MCC DAQ Quick Start for instructions on installing the software on the MCC DAQ CD. Refer to the device product page on the Measurement Computing website for information about the included and optional software supported by the USB-CTR04.

Install the software before you install your device

The driver needed to run the USB-CTR04 is installed with the software. Therefore, you need to install the software package you plan to use before you install the hardware.

Installing the hardware

To connect the USB-CTR04 to your system, connect the USB cable to an available USB port on the computer or to an external USB hub connected to the computer. Connect the other end of the cable to the USB connector on the device. No external power is required.

When connected for the first time, a **Found New Hardware** dialog opens when the operating system detects the device. When the dialog closes, the installation is complete. The **Status** LED turns on after the device is successfully installed (see Figure 2 on page 7).

If the Status LED turns off

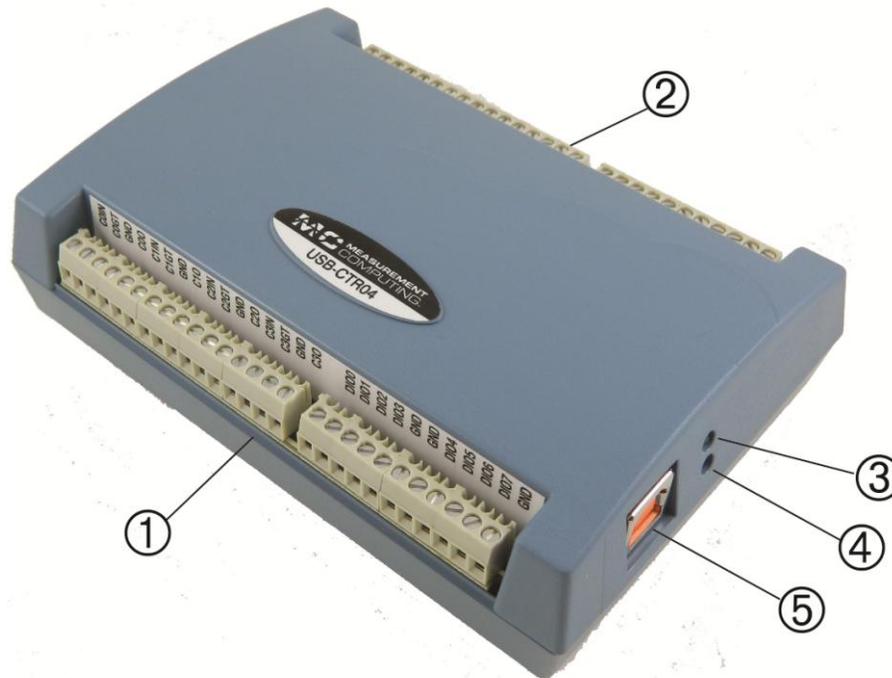
If communication is lost between the device and the computer, the **Status** LED turns off. To restore communication, disconnect the USB cable from the computer and then reconnect it. This should restore communication, and the **Status** LED should turn on.

Functional Details

External components

The USB-CTR04 has the following external components, as shown in Figure 2.

- Two screw terminal banks
- Device Status and Activity LEDs
- USB connector



- | | | | |
|---|--------------------------|---|---------------|
| 1 | Screw terminals 1 to 28 | 4 | Activity LED |
| 2 | Screw terminals 29 to 56 | 5 | USB connector |
| 3 | Status LED | | |

Figure 2. USB-CTR04 external components

Screw terminals

The device has two banks of screw terminals that provide the following connections:

- Four counter inputs
- Four counter outputs
- Four counter gates
- Eight DIO
- Four timer outputs
- External trigger input
- External clock input
- Internal clock output
- Power output
- Digital grounds

Counter input modes

The USB-CTR04 supports the following counter input modes:

- Totalize
- Period measurement
- Pulse-width measurement
- Timing measurement

Counter input modes are programmable with software. Some modes include software-selectable max limit and min limit register values. These values do not directly affect the current count, but set limits in some modes to determine counter behavior.

Each mode supports additional counter operation options. Refer to the discussion of each counter mode in the pages that follow for specific information.

Totalize mode

You can use the USB-CTR04 as a high speed pulse counter for general counting applications.

Each counter can be set to any resolution up to 64-bits based on the software-selectable max limit and min limit register values. The counters can accept frequency inputs up to 48 MHz.

In totalize mode, **CxIN** is used as the primary counter input. **CxGT** can be used to set the count direction, to gate the counter, to clear/reload the counter with the min limit value, or to trigger a particular counter to begin counting.

All totalize measurement mode options are software-selectable. Each option is explained in the table below.

Totalize counter mode options

Counter option	Description
Clear on read	The counter is cleared after each read (synchronous or asynchronous). The value of the counter before it was cleared is latched and returned. It is typically cleared to zero, but depending on counting mode, it may be cleared to the value stored in the min limit register.
Range Limit	When the range limit option is enabled, you can set the max limit and the min limit register values to mimic limit switches in a mechanical counter. <ul style="list-style-type: none"> ▪ When counting up, the counter freezes or rolls over to the min limit count whenever the count reaches the max limit register value. ▪ When counting down, the counter freezes or rolls over to the max limit count whenever the count reaches the min limit register value
Non-recycle	The counter freezes if the max limit or the min limit is reached. <ul style="list-style-type: none"> ▪ When counting up, the counter stops when the max limit is reached. ▪ When counting down, the counter stops when the min limit is reached. Counting resumes if the direction is reversed or if the counter is reloaded with a value between the max limit and the min limit.
CountDown	Enables count down mode. (This is overridden by the state of the gate input if the gate is programmed for direction control.)
Output On	Enables counter output mode. Based on the <i>output initial state</i> of the counter (high or low), the counter output toggles the state of the counter when it reaches the value of output register 0, and toggles back to output initial state of the counter when the it reaches the value of output register 1.
Output Initial State	Sets the initial state of the counter output to either high or low (default).

Totalize options that are specific to the counter gate signal (**CxGT**) are explained below.

Counter gate (CxGT) input mode options (Totalize mode)

Gate option	Description
Direction Control	Direction control allows CxIN to act as the pulse source and CxGT as the direction. By default, the counter increments when CxGT =1 (high), and decrements when CxGT =0 (low).
Gating	Gating allows the CxGT input to gate the counter. By default, the counter is enabled when the CxGT signal is high. When the CxGT signal is low the counter is disabled, but holds the count value.
Clear/Reload	Clears the count to zero unless counting in Range Limit mode. If counting in Range Limit mode, the CxGT signal reloads the counter from the min limit register.
Count Trigger	The counter starts counting when the CxGT input goes active. By default, active is on the rising edge.

Period measurement mode

You can use the USB-CTR04 to measure the period of any signal at a counter input (**CxIN**). The device counts the integral number of *ticks* that make up the period, and the data returned is always time measured in ticks.

Data sample errors come from two sources:

- the sampling error caused by not being able to count a partial tick
- the USB-CTR04 internal timebase inaccuracy.

The measurement period is the time from edge-to-edge, either both rising or both falling. Period data is latched as it becomes available, and is acquired at the counter read rate.

Because updates occur only when another full period becomes available:

- If the counter read period is *faster* than the input period, period values repeat in the acquisition. The bigger the difference between the counter read period and the input period, the more period values are repeated.
- If the counter read period is *slower* than the input period, then the acquisition misses some periods. The bigger the difference between the counter read period and the input period, the more period values are missed.

To obtain greater resolution, increase the counter read period, or use a period mode option.

The data returned is interpreted as time measured in ticks. This data represents the number of tick size intervals counted during the period measurement.

Optionally, you can use the counter gate signal (**CxGT**) to gate the counter.

- When **CxGT** is high, the counter is enabled.
- When **CxGT** is low, the counter is disabled, but holds the count value.

The 96 MHz system clock is used as the timing source. Periods from sub-microsecond to many seconds can be measured.

All period measurement mode options are software-selectable. Each period measurement option is explained in the table below.

Period option	Description
Period mode	X1 – The measurement is latched each time one complete period is observed. X10 – The measurement is latched each time 10 complete periods are observed. X100 – The measurement is latched each time 100 complete periods are observed X1000 – The measurement is latched each time 1000 complete periods are observed.
Tick size (period resolution)	The tick size is a fundamental unit of time derived from the period of the 96 MHz system clock. Four counter channel tick sizes are available – 20.83 ns, 208.3 ns, 2083.3 ns, and 20833.3 ns.

The USB-CTR04 internal timebase has an absolute accuracy of 30 ppm. The sampling error varies based on the input frequency, selected tick size, and selected period mode. The absolute error is the root-sum-of-squares of the two independent error sources.

Pulse width measurement mode

You can use the USB-CTR04 to measure the time from the rising edge to the falling edge, or vice versa, on a counter input signal (CxIN). The measurement is either pulse width low or pulse width high, depending upon the edge detection setting.

- If the counter read period is *faster* than the input period, pulse widths repeat in the acquisition. The bigger the difference between the counter read period and the input period, the more pulse widths are repeated.
- If the counter read period is *slower* than the input period, then the acquisition misses some pulse widths. The bigger the difference between the counter read period and the input period, the more pulse width values are missed.

Decrease the counter read period in order to increase the number of different pulse widths received.

Every time the pulse width measurement is latched from the counter, the counter is immediately cleared and enabled to count the time for the next pulse width. The pulse width measurements are latched as they become available.

The data returned is interpreted as time measured in ticks. This data represents the number of tick size intervals counted during the pulse width measurement.

Optionally, you can use the counter gate signal (**CxGT**) to gate the counter.

- When **CxGT** is high, the counter is enabled.
- When **CxGT** is low, the counter is disabled, but holds the count value.

The 96 MHz system clock is used as the timing source. Pulse widths from sub-microsecond to many seconds can be measured.

Pulse width measurement mode tick size options are software-selectable. The tick size is a fundamental unit of time derived from the period of the 96 MHz system clock.

Four counter channel tick sizes (pulse width resolutions) are available – 20.83 ns, 208.3 ns, 2083.3 ns, and 20833.3 ns.

Timing mode

You can use the USB-CTR04 to measure the time between an event on **CxIN** and a subsequent event on **CxGT**, such as the rising or falling edge of one event with respect to the rising or falling edge of another event (based on the edge detection setting).

Whenever the time measurement is latched from the counter, the counter is immediately cleared and enabled for accepting the subsequent time period, which starts with the next edge on the main channel.

The following example measures the time between the rising edge on a counter input (**CxIN**) and the falling edge on the counter gate (**CxGT**). The counter read operation returns zeroes until one complete time measurement has been taken. Then, the value (time in ticks) is latched by the device until the next time measurement is completed. At that time, rising edges on the counter input channel clear the counter and falling edges on the gate input latch the output of the counter.

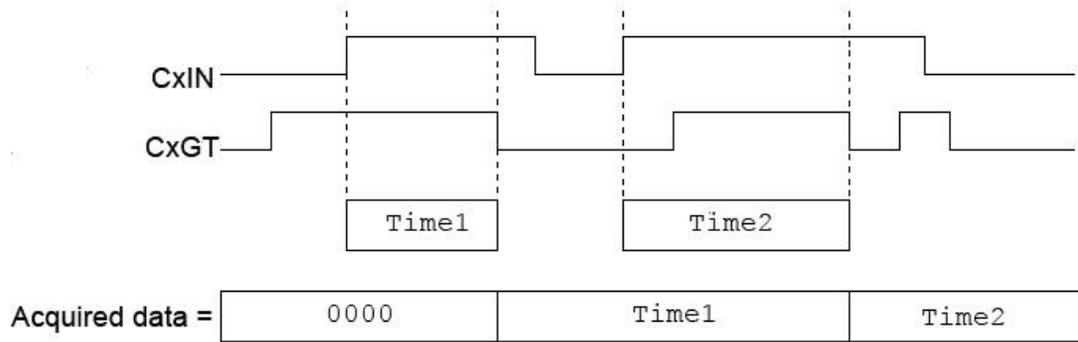


Figure 4. Counter input channel in timing mode

- If the counter read period is *faster* than the than the occurrence of the next time-frame rate (available on the two channels), then some time frames repeat in the acquisition. The bigger the difference between the counter read period and the time frame occurrence, the more time frames are repeated.
- If the counter read period is *slower* than the time-frame occurrence, then the acquisition misses some time frames. The bigger the difference between the counter read period and the time frame occurrence, the more time frames are missed.

Decrease the counter read period in order to capture more time frames.

The data returned is interpreted as time measured in ticks. This data represents the number of tick size intervals counted during the timing measurement.

Timing mode tick size options are software-selectable. The tick size is a fundamental unit of time derived from the period of the 96 MHz system clock.

Four counter channel tick sizes are available – 20.83 ns, 208.3 ns, 2083.3 ns, and 20833.3 ns.

Debounce filters

The USB-CTR04 has debounce circuitry which eliminates switch-induced transients that are typically associated with electro-mechanical devices including relays, proximity switches, and encoders.

All debounce filter options are software-selectable. You can select a debounce time, debounce mode, and rising-edge or falling-edge sensitivity. Each channel can be debounced with 16 programmable debounce times in the range of 500 ns to 25.5 ms.

Two debounce filter modes (*trigger after stable* and *trigger before stable*) and a debounce bypass are shown in Figure 5. The signal from the buffer can be inverted before it enters the debounce circuitry. The inverter is used to make the input rising-edge or falling-edge sensitive.

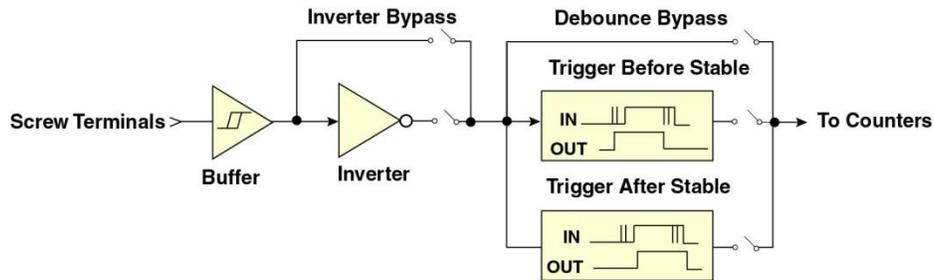


Figure 5. Debounce block diagram

Edge selection is available with or without debounce. In this case, the debounce time setting is ignored and the input signal goes straight from the inverter or inverter bypass to the counter module.

The two debounce filter modes are *trigger after stable* and *trigger before stable*. In either mode, the selected debounce time determines how fast the signal can change and still be recognized.

Trigger after stable mode

In the *trigger after stable* mode, the output of the debounce module does not change state until a period of stability has been achieved. This means that the input has an edge, and then must be stable for a period of time equal to the debounce time. Refer to Figure 6.

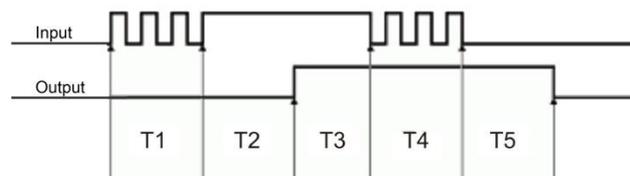


Figure 6. Trigger after stable mode

T1 through T5 indicate time periods. In trigger after stable mode, the input signal to the debounce module is required to have a period of stability after an incoming edge, in order for that edge to be accepted (passed through to the counter module). For this example, the debounce time is equal to T2 and T5.

- T1 – In Figure 6, the input signal goes high at the beginning of time period T1, but never stays high for a period of time equal to the debounce time setting (equal to T2 for this example.)
- T2 – At the end of time period T2, the input signal has transitioned high and stayed there for the required amount of time—therefore the output transitions high. If the input signal does not stabilize in the high state long enough, no transition would have appeared on the output and the entire disturbance on the input would have been rejected.
- T3 – During time period T3, the input signal remained steady. No change in output is seen.
- T4 – During time period T4, the input signal has more disturbances and does not stabilize in any state long enough. No change in the output is seen.
- T5 – At the end of time period T5, the input signal has transitioned low and stayed there for the required amount of time—therefore the output goes low.

Trigger before stable mode

In the *trigger before stable* mode, the output of the debounce module immediately changes state, but will not change state again until a period of stability has passed. For this reason the mode can be used to detect glitches. Refer to Figure 7.

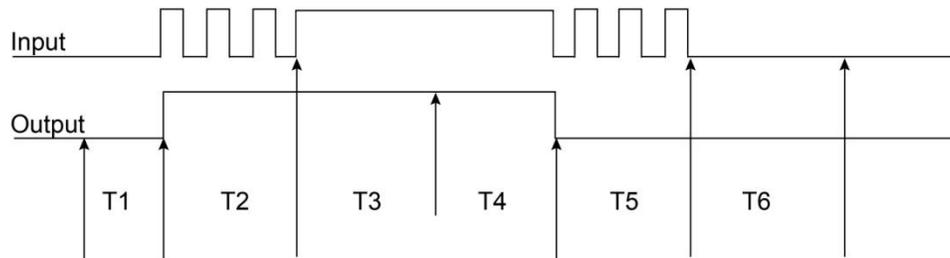


Figure 7. Trigger before stable mode

T1 through T5 in Figure 7 indicate time periods:

- T1 – The input signal is low for the debounce time (equal to T1); therefore when the input edge arrives at the end of time period T1, it is accepted and the output (of the debounce module) goes high. Note that a period of stability must precede the edge in order for the edge to be accepted.
- T2 – During time period T2, the input signal is not stable for a length of time equal to T1 (the debounce time setting for this example.) Therefore, the output stays "high" and does not change state during time period T2.
- T3 – During time period T3, the input signal is stable for a time period equal to T1, meeting the debounce requirement. The output is held at the high state. This is the same state as the input.
- T4 – At anytime during time period T4, the input can change state. When this happens, the output will also change state. At the end of time period T4, the input changes state, going low, and the output follows this action by going low.
- T5 – During time period T5, the input signal again has disturbances that cause the input to not meet the debounce time requirement. The output does not change state.
- T6 – After time period T6, the input signal has been stable for the debounce time, and therefore any edge on the input after time period T6 is immediately reflected in the output of the debounce module.

Debounce filter mode comparisons

Figure 8 shows how the two modes interpret an input signal, which exhibits glitches. Notice that the *trigger before stable* mode recognizes more glitches than the *trigger after stable* mode. Enable the **bypass** option in software to achieve maximum glitch recognition.

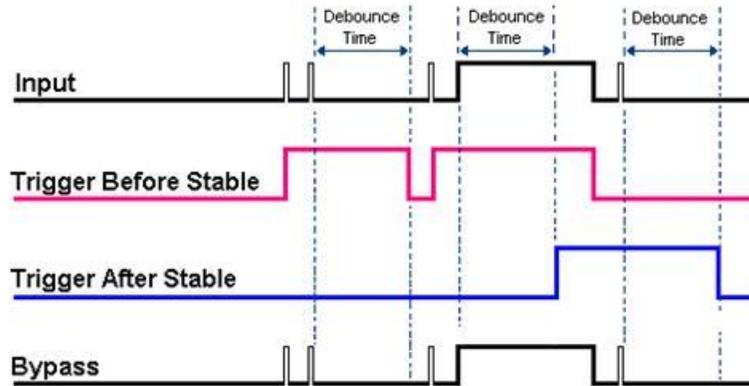


Figure 8. Example of two debounce modes interpreting the same signal

Set the debounce time according to the amount of instability expected in the input signal. Setting a debounce time that is too short may result in unwanted glitches clocking the counter. Setting a debounce time that is too long may result in an input signal being rejected entirely. Some experimentation may be required to find the appropriate debounce time for a particular application.

To see the effects of different debounce time settings, view the analog waveform along with the counter output. This can be done by connecting the source to an analog input.

Use *trigger before stable* mode when the input signal has groups of glitches and each group is to be counted as one. The trigger before stable mode recognizes and counts the first glitch within a group but rejects the subsequent glitches within the group if the debounce time is set accordingly. Set the debounce time to encompass one entire group of glitches, as shown in Figure 9.

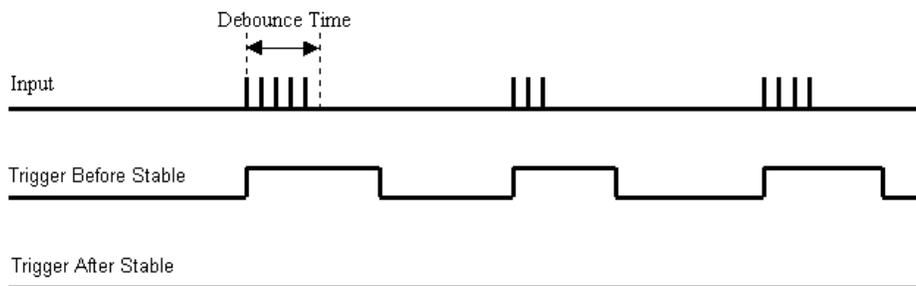


Figure 9. Optimal debounce time for trigger before stable mode

Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. *Trigger after stable* mode is used with electro-mechanical devices like encoders and mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving.

The debounce time should be set short enough to accept the desired input pulse but longer than the period of the undesired disturbance, as shown in Figure 10.

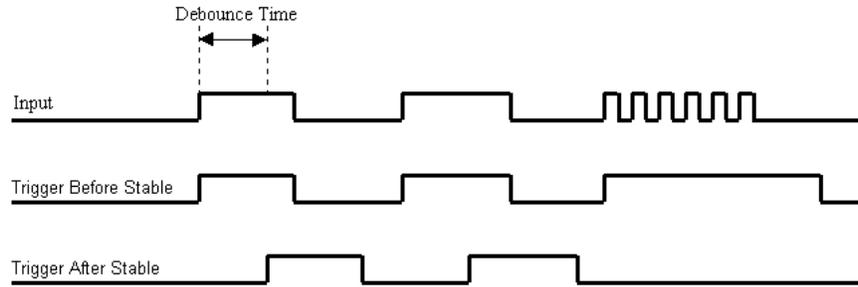


Figure 10. Optimal debounce time for trigger after stable mode

Digital I/O

You can connect up to eight digital I/O lines to **DIO0** through **DIO7**. The digital I/O terminals can detect the state of any TTL-level input. Refer to the schematic shown in Figure 11.

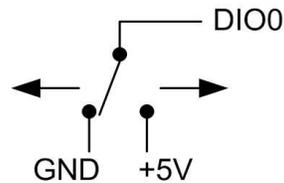


Figure 11. Schematic showing switch detection by digital channel DIO0

If you set the switch to the +5 V input, DIO0 reads *TRUE* (1). If you move the switch to GND, DIO0 reads *FALSE* (0).

Pull-up/down jumper

The digital port has 47 k Ω resistors that you can configure as pull-up or pull-down with internal jumper (see Figure 12 on page 16 for the location of this jumper).

Unconnected inputs are pulled low by default to 0 V through 47 k Ω resistors. The pull-up/pull-down voltage is common to all 47 k Ω resistors.

You must remove the cover from the device in order to access the jumper.

Caution! The discharge of static electricity can damage some electronic components. Before removing the device from its housing, either ground yourself using a wrist strap or touch the computer chassis or other grounded object to eliminate any stored static charge.

To open the case and set the pull-up/down jumper, complete the following steps:

1. Turn the device over and rest the top of the housing on a flat, stable surface.
2. Peel off the four rubber feet on the bottom of the device to access the screws.
3. Remove the four screws from the bottom of the device.
4. Hold both the top and bottom sections together, turn the device over and rest it on the surface, and then carefully remove the top section of the case to expose the circuit board.
5. Configure the jumper for either pull-up or pull-down. The jumper is configured by default for pull-down (see Figure 12 and Figure 13).

Figure 12 shows the location of the pull-up/down jumper on the USB-CTR04 with the enclosure removed.

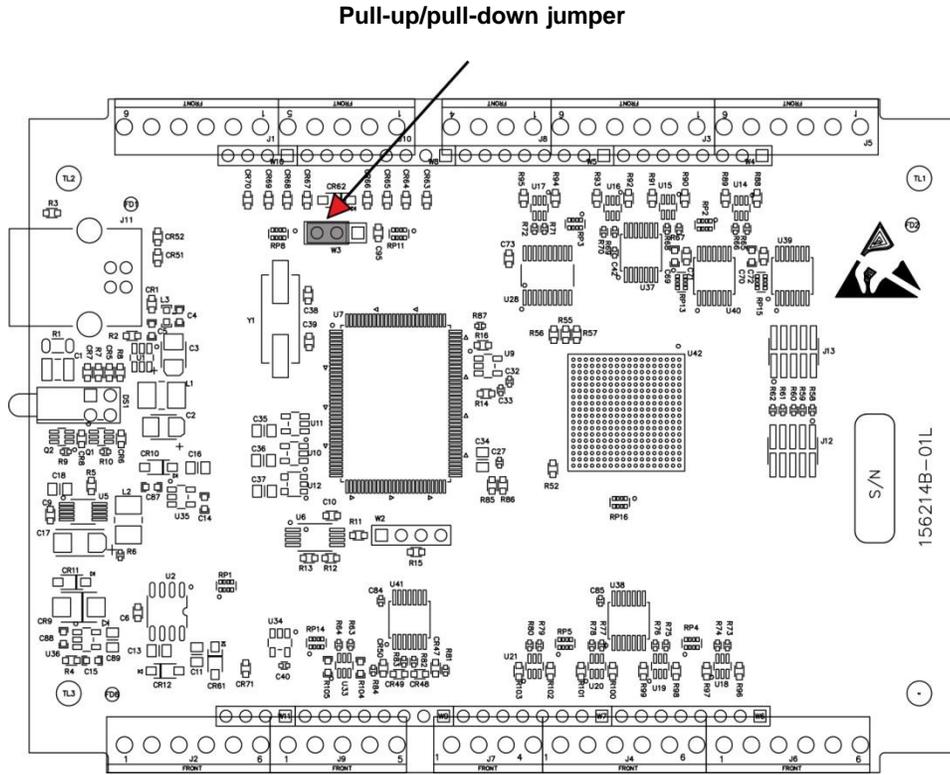


Figure 12. Pull-up/down jumper location

The pull-up/down jumper is configured by default for pull-down (see Figure 13).

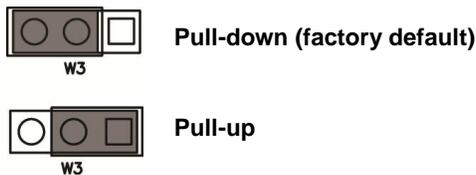


Figure 13. Pull-up/down jumper configurations

To pull the digital inputs high (5 V), configure the jumper for pull-up.

Proper LED alignment

When placing the circuit board within the housing, align the board LEDs with the top of the housing before attaching the housing bottom.

Timer output

You can use **TMR0** through **TMR3** as 32-bit timer outputs. Each timer can generate a programmable width pulse with a software-selectable frequency in the range of 0.022 Hz to 48 MHz. At higher frequencies, the timer output frequency and duty cycle depend on the load impedance and the supply.

The timer output rate and pulse width can be updated asynchronously at any time, however, doing so results in a pulse stream that is not seamless.

The following timer output options are software-selectable:

- pulse frequency
- duty cycle (pulse width divided by the pulse period)

- number of pulses to generate
- time delay before starting the timer output after it's enabled
- resting state of the output (*idle high* or *idle low*)

Both the period and time delay ranges are 20.83 ns to 44.739 seconds.

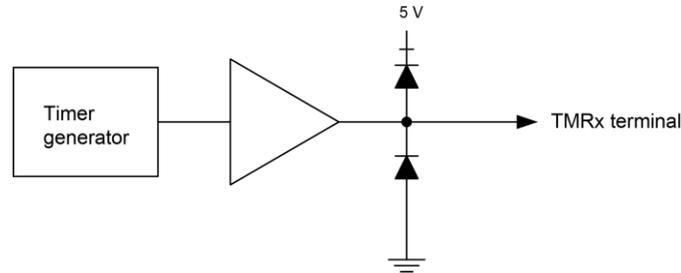


Figure 14. USB-CTR04 PWM timer channel

Trigger input

You can trigger synchronous acquisitions of counter data internally with software or externally using the **TRIG** digital trigger input screw terminal.

The **TRIG** input allows TTL-level triggering with latencies guaranteed to be less than 20.83 ns. The acquisition can be triggered on a rising or falling edge, or on a high or low level. The trigger input is TTL logic. Latency is one sample period, maximum. The input signal range is -0.5 V to 5.5 V maximum. The logic level (1 or 0) and the rising or falling edge for the discrete trigger input are software-selectable. You can set up a repetitive trigger mode with software; the trigger is automatically rearmed after it is activated.

When using the external trigger, the counter begins counting when the scan starts, even though acquisition of the count is held off by the trigger. To coordinate the start of acquisition with the start of the count, you could use the trigger signal to also trigger the gate of the counter in use. Clearing the counter before starting the scan will re-arm the gate trigger.

External clock pacing

You can pace synchronous acquisition of counter data by the onboard clock or by an external clock connected to the **CLKI** external clock input terminal.

Power

You can use the **+VO** power output terminal to supply power to external devices or circuitry.

Caution! The **+VO** terminal is an output. Do not connect to an external power supply or you may damage the USB-CTR04 and possibly the computer.

The maximum total output current that can be drawn from all USB-CTR04 connections (counter outputs, timer outputs, digital outputs, pacer clock output, and **+VO**) is 240 mA. This maximum applies to most personal computers and self-powered USB hubs. Bus-powered hubs and notebook computers may limit the maximum available output current to 100 mA.

If the current requirement of the device exceeds the current available from the computer, connect to a self-powered hub or power the computer with an external power adapter.

Ground

The ground (**GND**) connections provide a common ground for the digital, counter, and power connections.

Caution! Make sure that the signals are connected such that there is no potential between PC ground and signal ground.

Mechanical Drawings

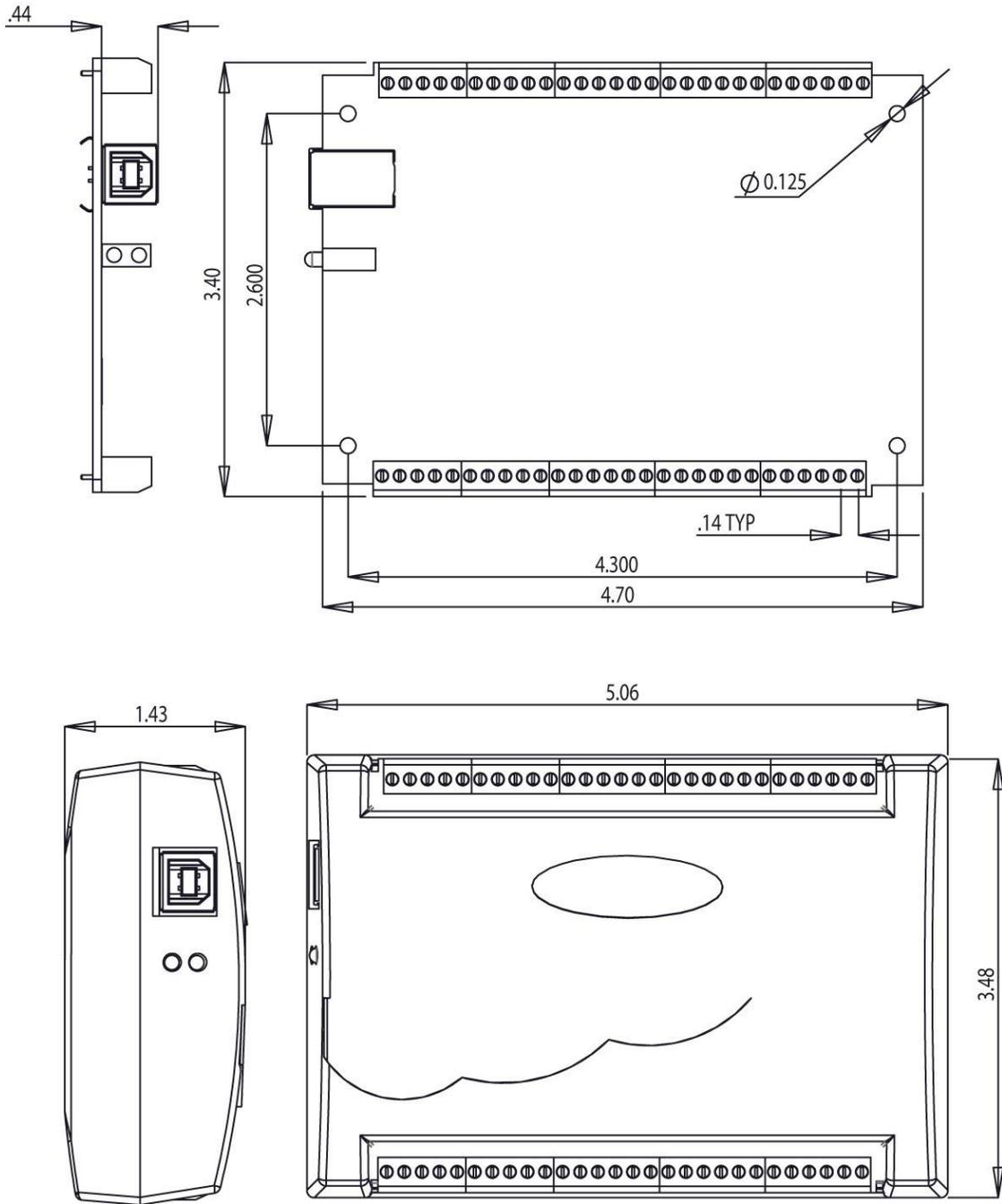


Figure 15. USB-CTR04 circuit board (top) and enclosure dimensions

Specifications

All specifications are subject to change without notice.

Typical for 25°C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Counter

Table 1. Counter specifications

Parameter	Specification
Counter type	FPGA
Counters	4 (each with a corresponding Input, Gate, and Output)
Counter input modes	Totalize, Pulse width, Period, Timing
Mode options	Non-Recycle, Range Limit, Clear on Read, Up/Down,
Gate options	Clear/Reload, Direction Control, Gate, Count trigger; mode dependent
Resolution	Up to 64-bits (software-selectable)
Maximum input frequency	48 MHz
Debounce times	16 steps from 500 ns to 25.5 ms; positive or negative edge sensitive; glitch detect mode or debounce mode; software-selectable.
Timebase and accuracy	96 MHz (24 MHz – 30 ppm with a 4x DLL (delay-locked loop))
Counter read pacer	Internal or external scan pacer up to 4 MHz
Period/pulse width resolution	20.83 ns; 208.3 ns; 2.083 μ s; or 20.83 μ s
Input type (C0IN to C3IN and C0GT to C3GT)	Schmitt trigger, 47 k Ω pull-down to ground with 33 Ω in series
Schmitt trigger hysteresis (C0IN to C3IN and C0GT to C3GT)	0.76 V typ 0.4 V min 1.2 V max
Input high voltage threshold (C0IN to C3IN and C0GT to C3GT)	1.74 V typ 1.3 V min 2.2 V max
Input high voltage limit (C0IN to C3IN and C0GT to C3GT)	5.5 V absolute max
Input low voltage threshold (C0IN to C3IN and C0GT to C3GT)	0.98 V typ 0.6 V min 1.5 V max
Input low voltage limit (C0IN to C3IN and C0GT to C3GT)	-0.5 V absolute min 0 V recommended min
Output high voltage	4.4 V min (IOH = -50 μ A) 3.76 V min (IOH = -24 mA)
Output low voltage	0.1 V max (IOL = 50 μ A) 0.44 V max (IOL = 24 mA)
Output current	24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

Timers

Table 2. Timer specifications

Parameter	Specification
Terminal names	TMR0, TMR1, TMR2, TMR3
Timer type	PWM output with count, period, delay, and pulse width registers
Output value	Default state is idle low with pulses high, software-selectable output invert
Internal clock frequency	96 MHz
Effective frequency range	0.022 Hz to 48 MHz
Register widths	32-bit
High pulse width	10.42 ns min
Low pulse width	10.42 ns min
Output high voltage	4.4 V min (IOH = -50 μ A) 3.76 V min (IOH = -24 mA)
Output low voltage	0.1 V max (IOL = 50 μ A) 0.44 V max (IOL = 24 mA)
Output current	24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

Digital input/output

Table 3. Digital input/output specifications

Parameter	Specification
Digital type	TTL
Number of I/O	8
Configuration	Bit-configurable as input (power on default) or output
Pull-up configuration	The port has a 47 k Ω resistor configurable as a pull-up or pull-down (default) with an internal jumper.
Digital I/O transfer rate (system-paced, asynchronous)	33 to 8000 port reads/writes or single bit reads/writes per second typical, system dependent.
Digital input pacing	Onboard clock, external input scan clock (CLKI)
Digital input trigger source	External single channel digital trigger (TRIG)
Input high voltage	2.0 V min 5.0 V absolute max
Input low voltage	0.8 V max 0 V recommended min
Output high voltage	4.4 V min (IOH = -50 μ A) 3.76 V min (IOH = -24 mA)
Output low voltage	0.1 V max (IOL = 50 μ A) 0.44 V max (IOL = 24 mA)
Output current	24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

External trigger

Table 4. Digital trigger specifications

Parameter	Specification
Trigger source	External digital; TRIG terminal
Trigger mode	Software-selectable for edge or level sensitive, rising or falling edge, high or low level.
Retrigger mode	Trigger is rearmed after each trigger event
Trigger latency	100 ns max
Trigger pulse width	100 ns min
Input type	Schmitt trigger, 47 k Ω pull-down to ground with 33 Ω in series
Schmitt trigger hysteresis	0.76 V typ 0.4 V min 1.2 V max
Input high voltage threshold	1.74 V typ 1.3 V min 2.2 V max
Input high voltage limit	5.5 V absolute max
Input low voltage threshold	0.98 V typ 0.6 V min 1.5 V max
Input low voltage limit	-0.5 V absolute min 0 V recommended min

External clock input/output

Table 5. External clock input/output specifications

Parameter	Specification
Terminal names	CLKI, CLKO
Terminal type	CLKI: Input, active on rising edge CLKO: Output, power on default is 0V, active on rising edge
Input clock frequency	4 MHz, max
Input clock pulse width	10.417 ns min
Input type	Schmitt trigger, 47 k Ω pull-down to ground with 33 Ω in series
Input Schmitt trigger hysteresis	0.76 V typ 0.4 V min 1.2 V max
Input high voltage threshold	1.74 V typ 1.3 V min 2.2 V max
Input high voltage limit	5.5 V absolute max
Input low voltage threshold	0.98 V typ 0.6 V min 1.5 V max
Input low voltage limit	-0.5 V absolute min 0 V recommended min
Output clock frequency	4 MHz, max
Output clock pulse width	10.417 ns
Output high voltage	4.4 V min (IOH = -50 μ A) 3.78V min (IOH = -24 mA)
Output low voltage	0.1 V max (IOL = 50 μ A) 0.44 V max (IOL = 24 mA)

Parameter	Specification
Output current	24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

Memory

Table 6. Memory specifications

Parameter	Specification
FIFO	8 KS
Non-volatile EEPROM	32 KB (10 KB firmware storage, 22 KB user data)

Power

Table 7. Power specifications

Parameter	Condition	Specification
Supply current, USB source	During enumeration	< 100 mA
	After USB enumeration	< 500 mA
+VO power available	After USB enumeration	5 V, $\pm 5\%$
+VO output current	After USB enumeration	24 mA max per pin, constrained to 240 mA across all output pins (counter outputs, timer outputs, digital outputs, pacer clock output, and +VO)

USB

Table 8. USB specifications

Parameter	Specification
USB device type	USB 2.0 (high-speed)
Device compatibility	USB 1.1, USB 2.0, USB 3.0
USB cable type	A-B cable, UL type AWM 2725 or equivalent. (min 24 AWG VBUS/GND, min 28 AWG D+/D-)
USB cable length	3 m (9.84 ft) max

Environmental

Table 9. Environmental specifications

Parameter	Specification
Operating temperature range	0 °C to 50 °C
Storage temperature range	-40 °C to 70 °C
Humidity	0% to 90% non-condensing

Mechanical

Table 10. Mechanical specifications

Parameter	Specification
Dimensions (L \times W \times H)	127 \times 89.9 \times 35.6 mm (5.00 \times 3.53 \times 1.40 in.)
User connection length	3 m (9.84 ft) max

Signal connector

Table 11. Screw terminal specifications

Parameter	Specification
Connector type	Screw terminal
Wire gauge range	16 AWG to 30 AWG

Screw terminal pinout

Table 12. Screw terminal pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	C0IN	Counter 0 input	28	N/C	No connection
2	C0GT	Counter 0 gate	29	N/C	No connection
3	GND	Digital ground	30	GND	Digital ground
4	C0O	Counter 0 output	31	N/C	No connection
5	C1IN	Counter 1 input	32	N/C	No connection
6	C1GT	Counter 1 gate	33	N/C	No connection
7	GND	Digital ground	34	GND	Digital ground
8	C1O	Counter 1 output	35	N/C	No connection
9	C2IN	Counter 2 input	36	N/C	No connection
10	C2GT	Counter 2 gate	37	N/C	No connection
11	GND	Digital ground	38	GND	Digital ground
12	C2O	Counter 2 output	39	N/C	No connection
13	C3IN	Counter 3 input	40	N/C	No connection
14	C3GT	Counter 3 gate	41	N/C	No connection
15	GND	Digital ground	42	GND	Digital ground
16	C3O	Counter 3 output	43	N/C	No connection
	Empty			Empty	
17	DIO0	DIO bit 0	44	TMR0	Timer 0 output
18	DIO1	DIO bit 1	45	TMR1	Timer 1 output
19	DIO2	DIO bit 2	46	GND	Digital ground
20	DIO3	DIO bit 3	47	TMR2	Timer 2 output
21	GND	Digital ground	48	TMR3	Timer 3 output
22	GND	Digital ground	49	TRIG	Trigger input
23	DIO4	DIO bit 4	50	GND	Digital ground
24	DIO5	DIO bit 5	51	CLKI	External clock input
25	DIO6	DIO bit 6	52	GND	Digital ground
26	DIO7	DIO bit 7	53	CLKO	Internal clock output
27	GND	Digital ground	54	+VO	User voltage output

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
Suite 1008
Norton, MA 02766
USA
Category: Electrical equipment for measurement, control and laboratory use.
Date of Issue: March 26, 2014

Measurement Computing Corporation declares under sole responsibility that the product

USB-CTR04

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: General Requirements, EN 61326-1:2006 + CRG:2011 / IEC 61326-1:2005.

Emissions:

- EN 55011:2009 + A1:2010 / CISPR 11:2009 + A1:2010: Radiated emissions: Group 1, Class A
- EN 55011:2009 + A1:2010 / CISPR 11:2009 + A1:2010: Conducted emissions: Group 1, Class A

Immunity: EN 61326-1:2006, Table 3.

- IEC 61000-4-2:2008: Electrostatic Discharge immunity.
- IEC 61000-4-3:2010: Radiated Electromagnetic Field immunity.
- To maintain compliance to the standards of this declaration, the following conditions must be met.
- The host computer, peripheral equipment, power sources, and expansion hardware must be CE compliant.
- All I/O cables must be shielded, with the shields connected to ground.
- I/O cables must be less than 3 meters (9.75 feet) in length.
- The host computer must be properly grounded.
- The host computer must be USB 2.0 compliant.
- Equipment must be operated in a controlled electromagnetic environment as defined by Standards EN 61326-1:2006, or IEC 61326-1:2005.

Note: Data acquisition equipment may exhibit noise or increased offsets when exposed to high RF fields (>1V/m) or transients.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in March, 2014. Test records are outlined in Chomerics Test Report #EMI6482.14

We hereby declare that the equipment specified conforms to the above Directives and Standards.



Carl Haapaoja, Director of Quality Assurance

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