CIO-DAS08/JR/16
&
CIO-DAS08/JR/16-AO

Analog and Digital I/O Board

User's Manual

Revision 4A
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1 INTRODUCTION

The CIO-DAS08/JR/16 combines analog inputs with digital input and output capability, while the CIO-DAS08/JR/16-AO version adds two channels of analog output capability. The CIO-DAS08/JR/16 may be upgraded to a CIO-DAS08/JR/16-AO by purchasing and installing the CIO-DUAL-DAC16 chip set.

1.1 DIGITAL OUTPUTS & INPUTS

There are eight inputs and eight outputs for sensing and controlling digital devices. They are port-addressable and are dedicated to either input or output. The digital outputs and inputs are TTL level.

1.2 ANALOG INPUTS AND OUTPUTS

The CIO-DAS08/JR/16 provides up to eight single-ended analog inputs. In addition to the inputs, the CIO-DAS08/JR/16-AO version can supply two analog voltage outputs. Sixteen-bit resolution is provided for analog inputs and outputs. The range is ±5V bipolar for analog inputs (and outputs if used).

2 SOFTWARE INSTALLATION

The board has a bank of switches and a jumper to set before installing the board in your computer. By far the simplest way to configure your board is to use the *Insta*Cal™ program provided as part of your software package. *Insta*Cal™ will show you all available options, how to configure the various switches and jumpers to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically know the exact configuration of the board.

Please refer to the *Software Installation Manual* regarding the installation and operation of *Insta*Cal. The following information is provided as a matter of completeness, and will allow you to do the hardware configuration of the board if you do not have immediate access to *Insta*Cal and/or your computer.

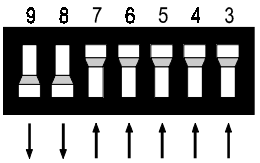
3 HARDWARE INSTALLATION

3.1 BASE ADDRESS

The base address of either versionof the CIO-DAS08/JR/16 is set by switching a bank of DIP switches. The bank of switches, labeled ADDRESS, is numbered 9 to 3.

Ignore the word ON and the numbers printed on the switch

Board logic adds up the weights of individual switches to determine the base address. A 'weight' is active when the switch is down. Shown to the right, switches 9 and 8 are down, all others are up. Weights 200h and 100h are active, totaling a 300h base address.



SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20
A4	10
A3	08

BASE ADDRESS SWITCH - Address 300H shown here.

Figure 3-1 Base Address Switches

Table 3-1. PC I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

3.2 SIMULTANEOUS TRANSFER JUMPER - CIO-DAS08/JR/16-AO Only

The analog outputs can be jumpered so that new output data are held until both DAC channels have been loaded with new digital data. Then, the new data updates the voltage outputs occurs when any addresses are read.

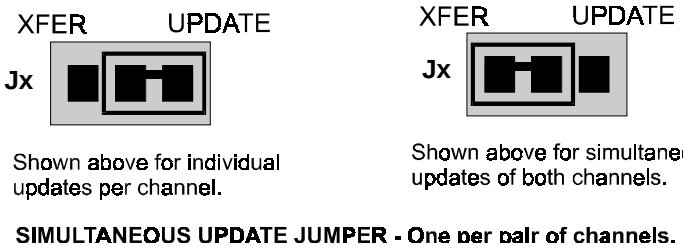


Figure 3-2. Simultaneous XFER/Individual UPDATE Jumper

A single jumper sets the DACs for either simultaneous transfer (XFER) or individual UPDATEs (Figure 3-2).

3.3 INSTALLING THE BOARD IN THE COMPUTER

1. Turn the power off.

2. Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

3. Locate an empty expansion slot in your computer.

4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DAS08/JR/16-AO.

4 CALIBRATION AND TEST

The board is supplied with software for calibration and test. You will find it in the InstaCal program under the CALIBRATE option. Follow the instructions to guide you through the calibration sequence.

5 SIGNAL CONNECTIONS

The I/O connector is a 37-pin, D-type connector accessible from the rear of the PC through the expansion backplate.

The connector accepts female 37-pin, D-type connectors, such as on the C37FF-2, a 2-foot cable with connectors. For quick and easy access to the board, use CIO-MINI37 screw terminal board.

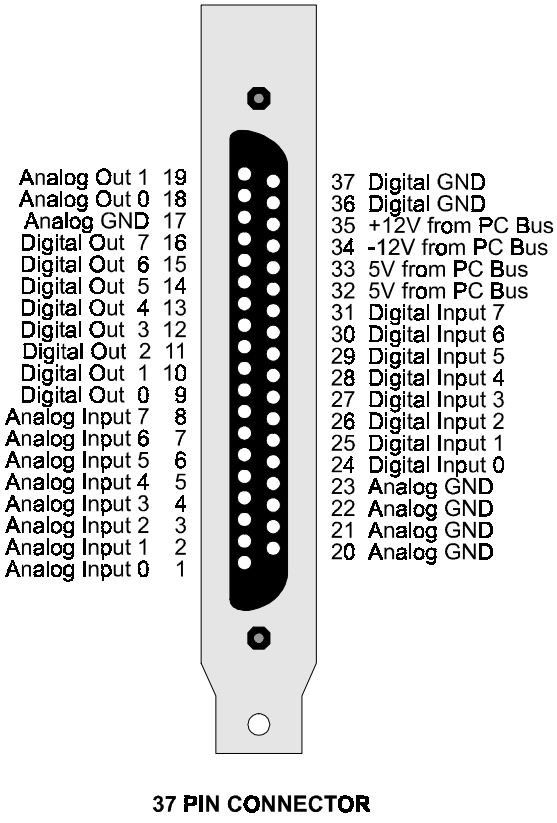


Figure 5-1. I/O Signal Connector - CIO-DAS08/JR/16-AO

NOTE: Pins 18 and 19 (Analog Out 0 and Analog Out 1) are not used in the CIO-DAS08/JR/16 board version.

6 REGISTER ARCHITECTURE

All of the programmable functions are accessible through the control and data registers, which are described here. We recommend programming with the Universal Library and not by direct register programming.

6.1 REGISTER LAYOUT

The board is controlled and monitored by writing to and/or reading from eight consecutive 8-bit I/O addresses. The first address, or BASE ADDRESS, is determined by setting a bank of DIP switches on the board.

A register is easy to read and write to. Most often, register manipulation is best left to ASSEMBLY language programs as most of the board's possible functions are implemented in easy to use Universal Library routines. Note that an X is an unspecified bit. There is no function associated with that bit position. All X bits should be masked out of reads.

To write to or read from a register in decimal or HEX, the following weights apply:

Table 6-1. Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

The registers and their function are listed on the following table. Within each register are 8 bits which may constitute a byte of data or eight individual bit set/read functions.

Table 6-2. Board Registers

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Bits 8 - 15 (LSB)	None
BASE + 1	A/D Bits 0 (MSB) - 7	Start 16 bit A/D conversion
BASE + 2	A/D status & MUX Address	Set A/D channel
BASE + 3	Digital input, 8 bits	Digital output, 8 bits
BASE + 4		D/A 0 LSB (CIO-DAS08/JR/16-AO only)
BASE + 5		D/A 0 MSB (CIO-DAS08/JR/16-AO only)
BASE + 6		D/A 1 LSB (CIO-DAS08/JR/16-AO only)
BASE + 7		D/A 1 MSB (CIO-DAS08/JR/16-AO only)

6.2 A/D DATA REGISTERS

BASE ADDRESS

7	6	5	4	3	2	1	0
A/D8	A/D9	A/D10	A/D11	A/D12	A/D13	A/D14	A/D15 LSB

READ ONLY

This register contains the least-significant eight bits of the analog input data from the A/D converter. These eight bits of analog input data are combined with the eight bits of analog input data in BASE + 1, forming a complete 16-bit number.
The data is in the format 0 = minus full scale. 65535 = +FS.

BASE ADDRESS + 1

7	6	5	4	3	2	1	0
POL/OVR MSB	A/D1	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7

READ: The most significant A/D byte is read.

WRITE: Any write to this register causes an immediate A/D conversion.
A note of caution: Read EOC between consecutive A/D conversions to avoid over-running the A/D converter.

POL/OVR: The POL/OVR bit indicates the polarity of the signal, and may be used to detect an overrange signal, and determine the value of that signal up to 192 counts over full scale.

To understand the operation of this bit, lets examine the process of making an A/D conversion.

1. To initiate a conversion, a write operation is performed on Base +1. The value of the data written does not matter. It is the toggling of the chip select line and the write signal that cause the conversion to start.

2. The End Of Conversion (EOC) bit must be monitored (bit 7, Base +2). To monitor this bit, read Base +2. Mask all but bit 7, and test for true (1) or false (0). While the bit is true, conversion is in progress. When it goes false the conversion is complete.

3. To read the converted signal value, read the LSB from Base +0 and the MSB from Base +1. The first time Base +1 is read, bit 7 will contain the polarity of the signal; true (1) for positive and false (0) for negative.

4. To check for an overrange condition, read Base +1 a second time. If bit 7 is true (1), the signal exceeds the full scale of the input. If false (0), the signal is within the range of the converter.

6.3 STATUS AND CONTROL REGISTER

BASE ADDRESS + 2

This address has two registers, one for reading and one for writing.

READ = STATUS

7	6	5	4	3	2	1	0
EOC	X	X	X	X	ChAdd2	ChAdd1	ChAdd0

EOC = 1 the A/D is busy converting and data should not be read.

EOC = 0 the A/D is not busy and data can be read.

ChAdd 2 to ChAdd 0 is the current analog input multiplexer channel. The current channel is a binary-coded number between 0 and 7.

WRITE = CONTROL

6		5	4	3	2	1	0
EOC	X	X	X	X	ChAdd2	ChAdd1	ChAdd0

ChAdd 2 to ChAdd 0. Set the current channel address by writing a binary-coded number between 0 and 7 to these three bits.

6.4 DIGITAL I/O CONTROL REGISTER

BASE ADDRESS + 3

This address contains two registers, one for outputs and one for inputs. The output register is latched and holds the last value written to it. The input register is not latched. Each time the register is read, the current state of the inputs is passed through this port into the computer.

WRITE = Set digital output port, all bits.

READ = Read digital input port, all bits, *and* update both D/As simultaneously with last values written to D/A output registers.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

6.5 D/A CONTROL REGISTERS (CIO-DAS08/JR/16-AO only)

Each D/A receives its data from a pair of 8-bit write-only registers. These registers contain the high byte and the low byte of the D/A 16-bit data word. The value written to these two registers determines the voltage output of the D/A chip. When in individual update mode, the D/A outputs are updated when the high byte for the channel is written.

When in simultaneous mode, the D/A outputs are updated with the values in the D/A output registers when any register from BASE +0 to BASE + 7 is read.

The D/A output range can generally be calculated as [(#/65536) * 10V] − 5V.

The #/65536 is a proportion of the Full Scale Range, which is +/-5V.

D/A 0 CONTROL REGISTERS

BASE ADDRESS + 4 DAC 0 LOW BYTE

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0 LSB

BASE ADDRESS + 5 DAC 0 HIGH BYTE

7	6	5	4	3	2	1	0
DA15 MSB	DA14	DA13	DA12	DA11	DA10	DA9	DA8

D/A 1 CONTROL REGISTERS

BASE ADDRESS + 6 DAC 1 LOW BYTE

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0 LSB

BASE ADDRESS + 7 DAC 1 HIGH BYTE

7	6	5	4	3	2	1	0
DA15 MSB	DA14	DA13	DA12	DA11	DA10	DA9	DA8

7 SPECIFICATIONS

ANALOG INPUTS - Both Versions

Type	TC-850 Integrating Converter
Resolution	16 bits, 65536 divisions of full scale
Number of Channels	8, single-ended
Range	±5V
A/D Conversion Time	30 ms
Throughput	30 Hz
Differential Linearity Error	± 0.5 LSB Max
Integral Linearity Error	± 1 LSB Max
No missing codes	Guaranteed to 16 bits
Voltage Reference Warm Up	20 Minutes Minimum 30 Minutes Typical
Input Leakage Current	100 nA max @ 25 deg. C.
On Channel Impedance	10 Megohms
Overvoltage	± 30 Volts Continuous

ANALOG OUTPUTS - CIO-DAS08/JR/16-AO Only

Type	AD660
Number of Channels	2
Range	± 5V Bipolar Only
Resolution	16 Bits (1/65536)
Settling time +/-FS	13 µs Max to +/-0.0008% of full scale
Linearity	± 2 LSB
Monotonicity	15 Bits guaranteed over temp range
Offset error	± 7mV
Gain error	± 3mV Max
Output Current	5 mA Min
Miscellaneous	Update DAC channels individually or simultaneously (jumper-selectable) Double-buffered latch output

DIGITAL I/O

Output Type	74LS373
Input Type	74LS244
Output low	0.4V max @ 8 mA
Output high	2.7V min @ –0.4 mA
IP1 - IP3 low	0.8V max, –0.5V absolute min
IP1 - IP3 high	2V min, 7V absolute max

ENVIRONMENTAL

Operating Temperature	0 to 50 deg C
Storage Temperature	–20 to 70 deg C
Humidity	0 to 90% non-condensing
Weight	5 oz

POWER CONSUMPTION - NO DACs

+5V Supply	310 mA typical / 510 mA max.
+12V Supply	25 mA typical / 36 mA max.
−12V Supply	16 mA typical / 25 mA max.

POWER CONSUMPTION - WITH DACs

+5V Supply	315 mA typical / 520 mA max.
+12V Supply	52 mA typical / 78 mA max.
−12V Supply	43 mA typical / 66 mA max.

NOTE Additional power will be drawn by user's connections to the power pins accessible on board connectors.

EC Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

Part Number	Description
CIO-DAS08/JR/16-AO	Analog I/O and Digital I/O board
CIO-DAS08/JR/16	Analog Input and Digital I/O board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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